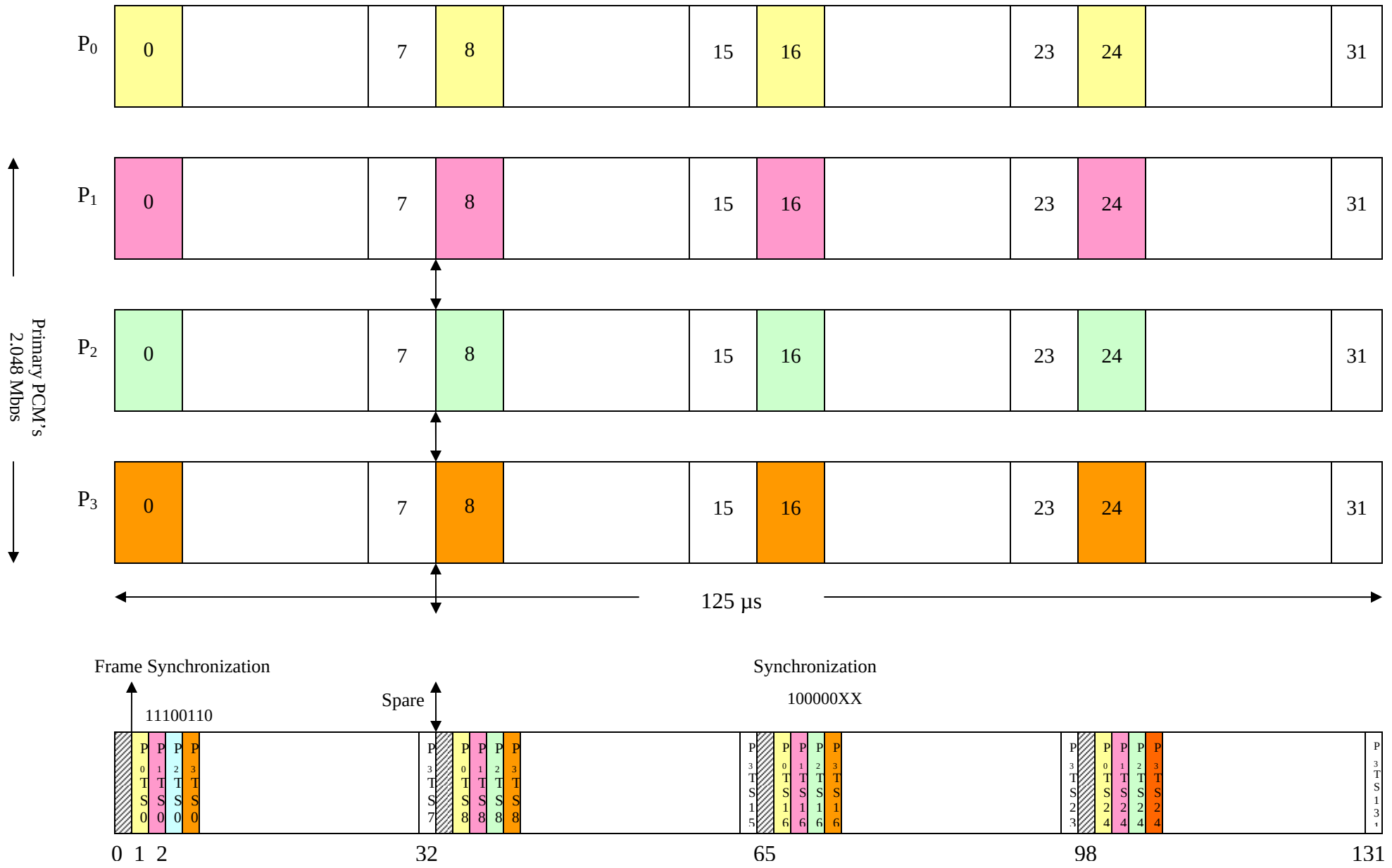
Practical PDH Higher Order Systems

Chapter 4

4.1 Examples of word interleaving

The following diagram shows how four primary PCM systems 2.048 are multiplexed into one higher order 8.448 Mbps. Here one should bear in mind that 64 bits are read in primary tributary, in the higher order PCM in addition to this 64 bits 2 bits will be sent. This means for every 8 time slots for four primary tributaries one time slot of 8 bits will be made in the higher order PCM in addition to all 8*4 time slots pertaining to the four primary PCM systems. It is easy to visualize this concept that is been deployed word interleaving as explained earlier.



8M BITS FRAME STRUCTURE
(Word Interleaving)
Figure: 4.1

Note: In 8Mbps PCM there are 132 TS in 125µs

4.2 Examples of Bit Interleaving

Bit interleaving is practically used in the Plesiochronous Digital Hierarchical system. When primary tributaries originating from different locations, reaching to a multiplexing location has undergone different technical and path conditions before arriving to the multiplexing location. Also these tributaries can have minute time differences of the clock pulses as well as minute differences of clock speed. All these primary PCMs has to be scanned or to be unified to a constant speed of a secondary PCM and after de-multiplexing the same timing characteristics should be maintained as the output of the de-multiplexer. How to analyze the differences of the primary tributary to be placed in the Higher Order PCM has to be analyzed for the practical PCM systems. This analysis is named as justification.

4.3 Justification

If f_p is the primary tributary speed and the secondary equivalent tributary speed is f_s.

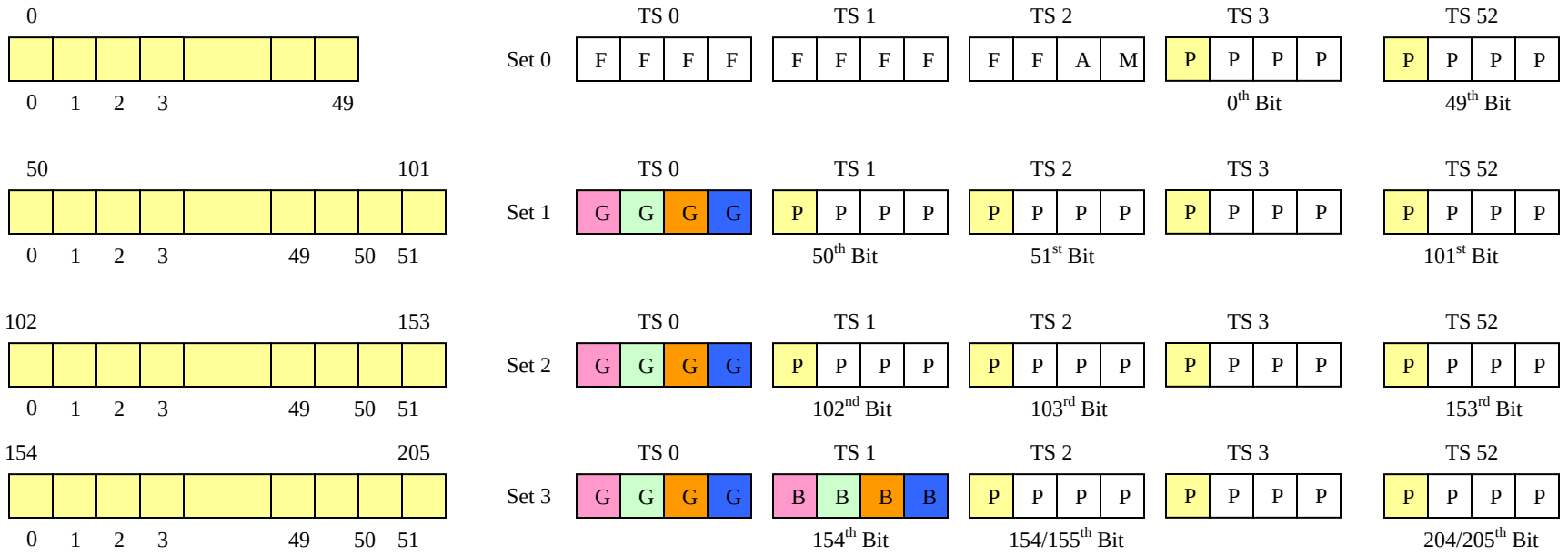
Ideally $f_p = f_s$ will result in no loss/addition of bits in the higher order PCM. This is named as Zero Justification. If $f_p > f_s$ there is a tendency to scan one primary bit as 2 secondary bits in the higher order. This is named as **Positive Justification**. In contrary if $f_p < f_s$ there is a tendency has one primary bit to be absent in the secondary tributary. This is named as **Negative Justification**.

But due to the introduction of bits at the multiplexing point ($f_p < f_s$) always in the PDH systems one can observe only Positive Justification..

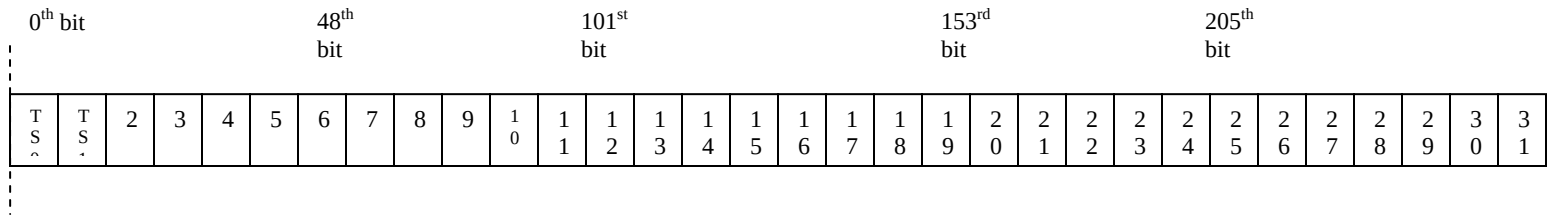
Let's assume 2.048 Mbps of primary Tributary has to be scanned in 2.112 Mbps into the secondary tributary (2.112= 8.448/4). This may lead to introduce one more bit into the higher order PCM when scanning more bits in the primary tributary. In the practical PDH systems of 2 to 8 Mbits a algorithm is utilized to verify whether bit is added in the secondary tributary as a false bit and this will be identified by testing four sets around 50 bits each set in 205 bits. This is shown as follows.

In one tributary take 50 bits and analyze whether there is a probability of introduction of an additional bit due to positive Justification, justification control bit pertaining to that tributary will be made positive (1). Then the second set pertaining to that tributary is again analyzed for positive justification and the probability is noted in the second justification control bits either one or zero depending up on the likelihood of introduction of a additional bit,. A similar exercise will be carried out for the third set of bits and accordingly justification control bit s will be made one or zero.

All these Justification Control bits resulting in majority of ones will indicate not to consider 155^{th} bit (justified timeslots) to be ignored by the de-multiplexer when de-multiplexing to the primary tributary. This is illustrated as follows.



If we consider one PCM Hence total of 205/206 bits will be taken from each PCM. Note: Of we start with bit No. 0, total of 204 or 205 will be taken)



Please note only PCM 0 has been indicated in color and other PCMs are not shown any color. For PCM 0, 1, 2 and 3 justification control bits and justified bits (154th time slot) are indicated in respectively. If set 1, set 2, Set 3 justification Control bits are 101 G respectively then 155th bit B Is ignored.

Or another example
If Justification Control Bits are 001 respectively 155th bit will be an actual bit.

Figure: 4.2

If the majority of the Justification Control bits are Ones the output of de-multiplexer will be sending only 204 bits while for another tributary with the majority of justification control bits are zero the output of the de-multiplexer will be sending 205 bits. So that the speed of the primary tributaries will be maintained after the Higher Order De-multiplexing.