Higher Order Path Overhead

There are 9 words for POH, which are listed below:

J1	Path trace - connection verification
B3	Path bit interleaved parity (BIP-8) - parity computed over previous container
C2	Path signal label – mapping type in VC-n
G1	Path status – monitoring of bidirectional path status
F2	Path user channel – 64 kbit/s user channel for operators
H4	Tributary unit multiframe indicator - start of multiframe
F3	Path user channel – 64 kbit/s user channel for operators
K3	Automatic Protection Switching (APS) – path protection
N1	Network operator byte – higher order tandem connection overhead (TCOH)

Details of J1 & B3 of Higher Order POH

- **J1 - Higher-Order VC-N path trace byte**
  This user-programmable byte repetitively transmits a 15-byte string plus 1-byte CRC-7. A 64-byte free-format string is also permitted for this Access Point Identifier. This allows the receiving terminal in a path to verify its continued connection to the intended transmitting terminal.
- **B3 - Path Bit Interleaved Parity code (Path BIP-8) byte**
  This is an even-parity code, used to determine if a transmission error has occurred over a path. Its value is calculated over all the bits of the previous virtual container before scrambling and placed in the B3 byte of the current frame. (BIP-8 is calculated on the 8 bit blocks of the n^{th} frame and placed on the $(n+1)^{th}$ frame of VC3/ VC4.)

What is BIP?

- Bit Interleaved Parity
- Error monitoring in SDH uses a CRC with a polynomial, xn+x0, called Bit Interleaved Parity (BIP-n).
- The signal to be monitored is divided in to small blocks with n-bit size. The even parity check is applied to each bit of all the blocks in the signal, fro m 1st to nth bit independently.

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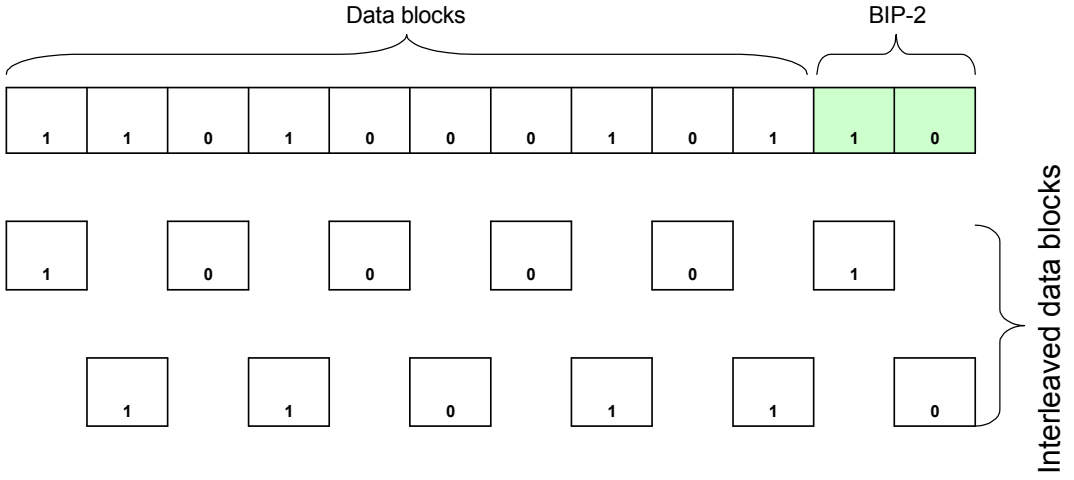
Example of BIP

- The following is an illustration of BIP-2 on a bit stream of 10 information bits and 2 even parity bits.



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Application of BIP in SDH Systems

Following table gives the varying values of n used at different stages of the multiplexing of an SDH signal

Frame	Order of BIP (n)	Reference abbreviation to the Overhead Byte
RSOH	BIP-8	B1
MSOH	BIP-24	B2
VC-4	BIP-8	B3
VC-3	BIP-8	B3
VC-12	BIP-2	V5 (b1,b2)

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Details of C2 of Higher Order POH

- **C2 - Path signal label byte** – This byte specifies whether the virtual container is equipped or not and the mapping type in the respective virtual container. Standard binary values for C2 are:

MSB	LSB	Hex Code	Interpretation
Bits 1-4	Bits	5-8	
0000	0000	00	Unequipped or supervisory-unequipped
0000	0001	01	Equipped – non-specific
0000	0010	02	TUG structure
0000	0011	03	Locked TU-n
0000	0100	04	Asynchronous mapping of 34,368 kbit/s or 44,736 kbit/s into the Container-3
0001	0010	12	Asynchronous mapping of 139,264 kbit/s into the Container-4
0001	0011	13	ATM mapping
0001	0100	14	MAN DQDB (IEEE Standard 802.6) mapping
0001	0101	15	FDDI (ISO Standard 9314) mapping
0001	0110	16	Mapping of HDLC/PPP (Internet Standard 51) framed signal
0001	0111	17	Mapping of Simple Data Link (SDL) with SDH self synchronising scrambler
0001	1000	18	Mapping of HDLC/LAP-S framed signals
0001	1001	19	Mapping of Simple Data Link (SDL) with set-reset scrambler
0001	1010	1A	Mapping of 10 Gbit/s Ethernet frames (IEEE 802.3)
1100	1111	CF	Obsolete mapping of HDLC/PPP framed signal
1110	0001	E1	Reserved for national use
:	:	:	:
1111	1100	FC	Reserved for national use
1111	1110	FE	Test signal, O.181 specific mapping
1111	1111	FF	VC-AIS

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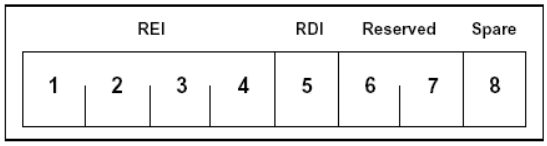
Details of G1 of Higher Order POH

- **G1 - Path status byte** – This byte is used to convey the path terminating status and performance back to the originating path terminating equipment. Therefore the bi-directional path in its entirety can be monitored, from either end of the path.



Byte G1 is allocated to convey back to a VC-4-Xc/VC-4/VC-3 trail termination source the status and performance of the complete trail. Bits 5 to 7 may be used to provide an enhanced remote defect indication with additional differentiation between the payload defect (PLM), server defects (AIS, LOP) and connectivity defects (TIM, UNEQ). The following codes are used:

Bits 5-7	Meaning	Triggers
001	No remote defect	No remote defect
010	E-RDI Payload defect	PLM
101	E-RDI Server defect	AIS, LOP
110	E-RDI Connectivity defect	TIM, UNEQ

REI – Remote Error Indicator (for path) An indication returned to a transmitting node (source) that an errored block has been detected at the receiving node (sink). REI was previously known as Far End Block Error (FEBE).

RDI – Remote Defect Indicator (for terminal)

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Details of G1 of Higher Order POH

(contd.)

- The E-RDI G1 (bits 5-7) code interpretation provides for interworking with equipment which supports RDI. It is not necessary for the interpretation to identify if the equipment supports RDI or E-RDI. For the E-RDI codes, bit 7 is set to the inverse of bit 6. Following is the E-RDI G1 (bits 5-7) code interpretation:

Bits 5-7	E-RDI Interpretation
000	No remote defect (Note 1)
001	No remote defect
010	E-RDI Payload defect (Note 2)
011	No remote defect (Note 1)
100	E-RDI Server defect (Note 1)
101	Remote E-RDI Server defect
110	Remote E-RDI Connectivity defect
111	Remote E-RDI Server Defect (Note 1)

NOTE 1: These codes are generated by RDI supporting equipment and are interpreted by E-RDI supporting equipment as shown. For equipment supporting RDI, clause 9.3.1.4/G.707, this code is triggered by the presence or absence of one of the following defects: AIS, LOP, TIM, or UNEQ. Equipment conforming to an earlier version of this standard may include PLM as a trigger condition. ATM equipment complying with the 1993 version of ITU-T Recommendation I.432 may include LCD as a trigger condition. Note that for some national networks, this code was triggered only by an AIS or LOP defect.

NOTE 2: ATM equipment complying with the 08/96 version of ITU-T Recommendation I.432.2 may include LCD as a trigger condition.

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Details of F2, H4, F3 & K3 of Higher Order POH

- F2 – Path user channel byte – This byte is used for user communication between path elements.
- H4 – Position and Sequence Indicator byte – This byte provides a multi frame and sequence indicator for virtual VC-3/4 concatenation and a generalized position indicator for payloads. In the latter case, the content is payload specific (e.g., H4 can be used as a multiframe indicator for VC-2/1 payload). For mapping of DQDB in VC-4, the H4 byte carries the slot boundary information and the Link Status Signal (LSS). Bits 1-2 are used for the LSS code as described in IEEE Standard 802.6. Bits 3-8 form the slot offset indicator. The slot offset indicator contains a binary number indicating the offset in octets between the H4 octet and the first slot boundary following the H4 octet. The valid range of the slot offset indicator value is 0 to 52. A received value of 53 to 63 corresponds to an error condition.
- F3 - Path user channel byte – This byte is allocated for communication purposes between path elements and is payload dependent.
- K3 - APS signalling is provided in K3 bits 1-4, allocated for protection at the VC-4/3 path levels. K3 bits 5-8 are allocated for future use. These bits have no defined value. The receiver is required to ignore their content.

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Details of N1 of Higher Order POH

- N1 - Network operator byte – This byte is allocated to provide a Higher-Order Tandem Connection Monitoring (HO-TCM) function. N1 is allocated for Tandem Connection Monitoring for contiguous concatenated VC-4, the VC-4 and VC-3 levels.

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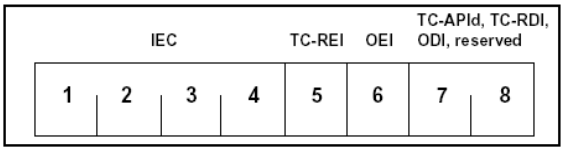
Details of N1 of Higher Order POH

(contd.)



Bits 1-4	Incoming Error Count (IEC).
1001	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1110	Incoming AIS

NOTE: To guarantee a non all-zeroes N1 byte independent of the incoming signal status, it is required that the IEC code field contains at least one “1”. When zero errors in the BIP-8 of the incoming signal are detected, an IEC code is inserted with “1”s in it. In this manner, it is possible for the Tandem Connection sink at the tail end of the Tandem Connection link to use the IEC code field to distinguish between unequipped conditions started within or before the Tandem Connection.

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Details of N1 of Higher Order POH

(contd.)

- Bit 5 - Operates as the TC-REI of the Tandem Connection to indicate errored blocks caused within the Tandem Connection.
- Bit 6 - Operates as the OEI to indicate errored blocks of the egressing VC-n.
- Bit 7,8 - Operate in a 76 multiframe as:
  - Access point identifier of the Tandem Connection (TC-APId); it complies with the generic 16-byte string format given in 9.2.2.2.
  - TC-RDI, indicating to the far end that defects have been detected within the Tandem Connection at the near end Tandem Connection sink.
  - ODI, indicating to the far end that AU/TU-AIS has been inserted into the egressing AU-n/TU-n at the TC-sink due to defects before or within the Tandem Connection.
  - Reserved capacity (for future standardization).

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Details of N1 of Higher Order POH

(contd.)

Frame #	Bits 7-8 definition
1-8	Frame Alignment Signal: 1111 1111 1111 1110
9-12	TC-APId byte #1 [1 $C_1C_2C_3C_4C_5C_6C_7$]
13-16	TC-APId byte #2 [0 X X X X X X X]
17-20	TC-APId byte #3 [0 X X X X X X X]
:	:
65-68	TC-APId byte #15 [0 X X X X X X X]
69-72	TC-APId byte #16 [0 X X X X X X X]
73-76	TC-RDI, ODI and Reserved (see following)

Frame #	Bit 7 definition	Bit 8 definition
73	Reserved (default = "0")	TC-RDI
74	ODI	Reserved (default = "0")
75	Reserved (default = "0")	Reserved (default = "0")
76	Reserved (default = "0")	Reserved (default = "0")

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Structure of TU12

The structure of TU3 is such that in a given 125μs frame when mapped directly from 34Mbps to VC3 and then to TU3 there are enough spare words to accommodate the POH and Pointer. However in the case of 2Mbps the number of spare words to accommodate POH and Pointer in a given 125μs period is not sufficient enough. Hence 4 frames of 125μs are used to indicate the POH and Pointer for the respective 2Mbps PDH stream. The slide shows how the POH is accommodated for 2Mbps tributary streams:

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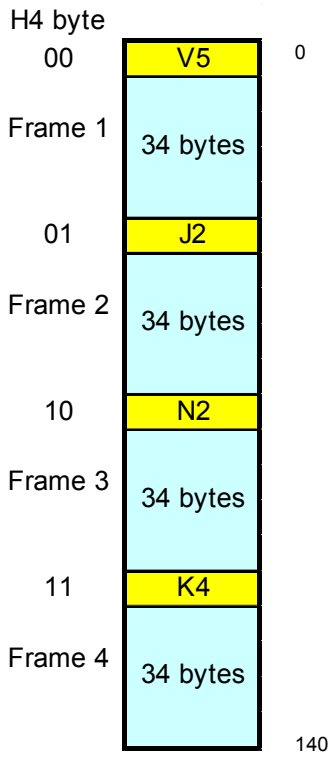
The Structure of VC12 POH



4 consecutive frames form a Multiframe

125*4 = 500 μs

Indication in H4 (Multiframe Indication Byte)

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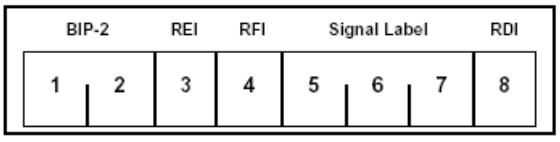
Details of V5 of Lower Order POH

- V5 – VT path overhead



Bits 1-2 Allocated for error performance monitoring. A Bit Interleaved Parity (BIP-2) scheme is specified. Includes POH bytes, but excludes V1, V2, V3, and V4.

Bit 3 A VC-2/VC-1 path Remote Error Indication (LP-REI) that is set to one and sent back towards a VC-2/VC-1 path originator if one or more errors were detected by the BIP-2; otherwise set to zero.

Bit 4 A VC-2/VC-1 path Remote Failure Indication (LP-RFI). This bit is set to one if a failure is declared, otherwise it is set to zero. A failure is a defect that persists beyond the maximum time allocated to the transmission system protection mechanisms.

Bits 5-7 Provide a VC-2/VC-1 signal label. The Virtual Container path Signal Label coding is:

- 000 Unequipped or supervisory-unequipped
- 001 Equipped – non-specific
- 010 Asynchronous
- 011 Bit synchronous
- 100 Byte synchronous
- 101 Reserved for future use
- 110 Test signal, O.181 specific mapping
- 111 VC-AIS

Bit 8 Set to 1 to indicate a VC-2/VC-1 path Remote Defect Indication (LP-RDI); otherwise set to zero.

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Details of J2 of Lower Order POH

- J2 - Used to repetitively transmit a Lower-Order Access Path Identifier so that a path receiving terminal can verify its continued connection to the intended transmitter. A 16-byte frame is defined for the transmission of Path Access Point Identifiers. This 16-byte frame is identical to the 16-byte frame of the J1 and J0 bytes.

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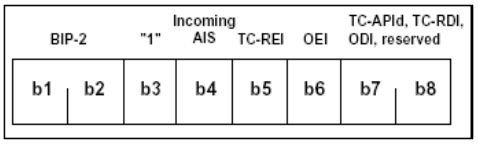
Details of N2 of Lower Order POH

(contd.)

- N2 - Allocated for Tandem Connection Monitoring for the VC2, VC-12, and VC-11 level.



Bits 1-2 Used as an even BIP-2 for the Tandem Connection.

Bit 3 Fixed to "1". This guarantees that the contents of N2 is not all zeroes at the TC- source. This enables the detection of an unequipped or supervisory unequipped signal at the Tandem Connection sink without the need of monitoring further OH-bytes.

Bit 4 Operates as an "incoming AIS" indicator.

Bit 5 Operates as the TC-REI of the Tandem Connection to indicate errored blocks caused within the Tandem Connection.

Bit 6 Operates as the OEI to indicate errored blocks of the egressing VC-n.

Bits 7-8 Operate in a 76 multiframe as:
– The access point identifier of the Tandem Connection (TC-APId)
– The TC-RDI, indicating to the far end that defects have been detected within the Tandem Connection at the near end Tandem Connection sink.
– The ODI, indicating to the far end that TU-AIS has been inserted at the TC-sink into the egressing TU-n due to defects before or within the Tandem Connection.
– Reserved capacity (for future standardization).

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Details of N2 of Lower Order POH

(contd.)

Frame #	Bits 7-8 definition
1-8	Frame Alignment Signal: 1111 1111 1111 1110
9-12	TC-APId byte #1 [1 $C_1C_2C_3C_4C_5C_6C_7$]
13-16	TC-APId byte #2 [0 X X X X X X X]
17-20	TC-APId byte #3 [0 X X X X X X X]
:	:
65-68	TC-APId byte #15 [0 X X X X X X X]
69-72	TC-APId byte #16 [0 X X X X X X X]
73-76	TC-RDI, ODI and Reserved (see following)

Frame #	Bit 7 definition	Bit 8 definition
73	Reserved (default = "0")	TC-RDI
74	ODI	Reserved (default = "0")
75	Reserved (default = "0")	Reserved (default = "0")
76	Reserved (default = "0")	Reserved (default = "0")

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Details of K4 of Lower Order POH

- K4 - Bits 1-4 are allocated for APS signalling for protection at the Lower-Order path level. Bits 5-7 are reserved for optional use. Bit 8 is reserved for future use and has no defined value.

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Comparison of POH in Higher and Lower Orders

Function	VC3,4 POH Byte	VC12 POH Byte
verification of VC connection	J1	J2
Bit Interleaved parity Check Byte	B3	V5(b1-b2)
Indication of VC composition	C2	V5(b5-b7)
Remote Alarm Indication	G1	V5(b3,4,8)
64kb clear channels	F2,F3	N/A
Multiframe Position Indicator	H4	N/A
Automatic Protection Switch signaling	K3	K4
Network Operator Byte	N1	N2
Spare (unused)		

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Pointers

- Application of Pointer
  - A Pointer is used to address a particular location within an AU or a TU structure. There are mainly 2 types of pointers
    1. AU Pointers: used to point at Higher Order VC's (VC-4,3) in an STM frame
    2. TU Pointers: used to point at Lower Order VC's (VC-12) in higher order VC

    Each of these pointers carry the offset number (address) at which the 1st byte of the payload is located, within the frame. The offset numbering of AU4, TU3, TU12, frames are shown in slide # 66, 68, 71. The offset numbering of TUs/AUs will be according to the CCITT Rec. G.707.

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Functions of a Pointer

- 1. Minimization of multiplexing Delay
  - This is the main advantage of pointers. Normally signals from different originating points differ in their phases, because of different transmission length and different clock generation. In the usual multiplexing process, to align them, each signal has to be written into memories and read out using a new phase of the frame to be multiplexed. Thus, it is inevitable to cause additional delay of half of the frame time in average and one frame time at maximum. Also, it requires large capacity memories.
  - To avoid above inconveniences, this pointer method was introduced into the multiplexing of SDH signal. A pointer is assigned to each VC to be multiplexed and it indicates relative phase shift between the VC and the new frame by using the address number in the new frame. As a matter of course, every VC has different pointer value. The pointer is renewed at every multiplexing process, so it is not necessary to introduce undesirable additional delays.
- 2. Frequency Justification
  - Generally this function is not required in an SDH network since all network elements are synchronized to a single clock. But if the VC's are transported over different networks, and if a network element is in an abnormal condition, justification is necessary to absorb any frequency differences between payload and the frames. There are 2 types of justification in SDH:

    a. Positive Justification: If the frame speed of the STM is higher than the payload arrival speed.

    b. Negative justification: If the frame speed of the STM is lower than the payload arrival speed.

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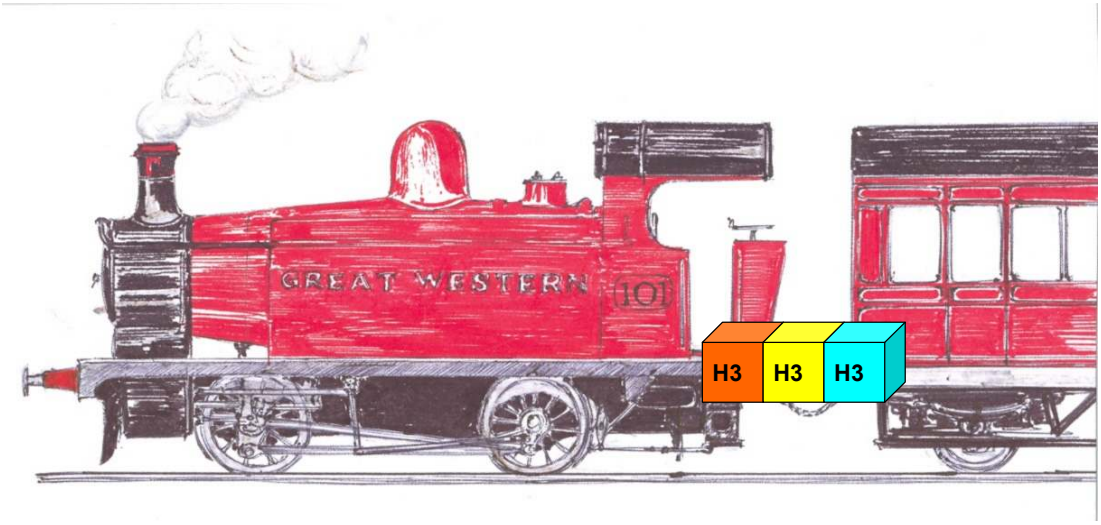
Positive justification



Application of the chain in the Train analogy.

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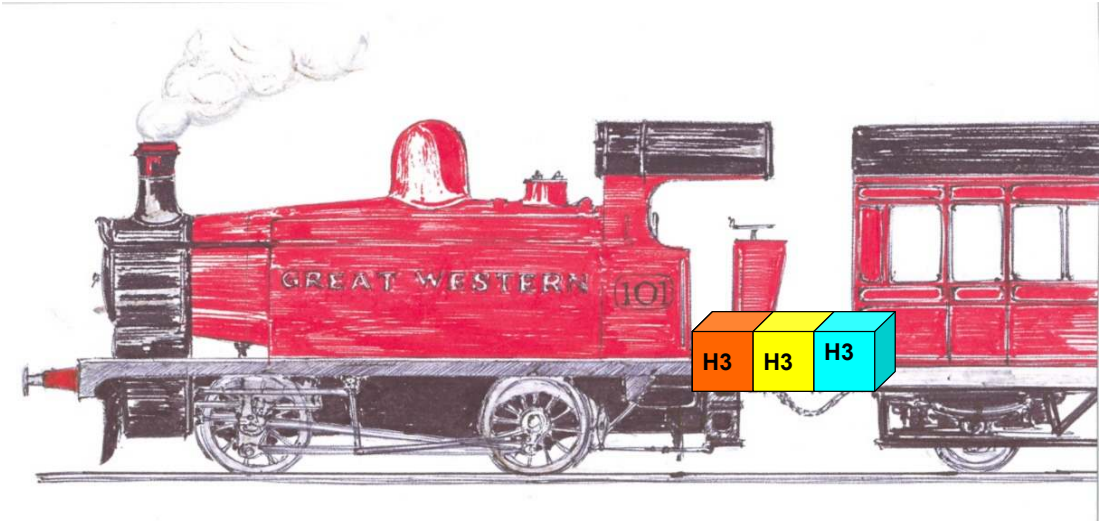
Negative justification



Application of the buffer in the Train analogy.

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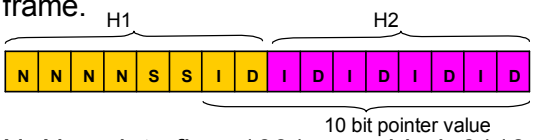
AU-4 Pointer

- This pointer points to the VC-4 in an STM-1 frame. Following is the typical structure of an AU-4 pointer.

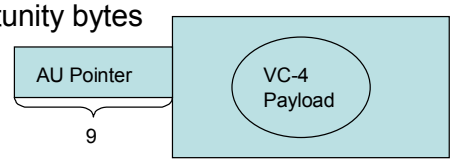
H1	Y	Y	H2	1*	1*	H3	H3	H3

- H1, H2 – Together are used to give the offset of the VC-4 in the STM-1 frame.



- N- New data flag, 1001 – enabled, 0110 – disabled
- I – Increment bit, In positive justification ‘I’ bits are inverted
- D – Decrement bit, In negative justification D bits are inverted.
- SS – 10

- H3 – Negative justification opportunity bytes
- Y – 1001SS11
- 1* - all 1 bits



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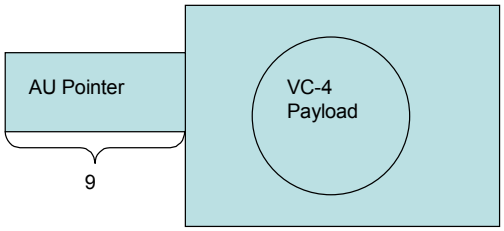
AU Pointer



Observations:

•When the payload is directly filled by 140 Mbps PDH an AU pointer will direct to the starting point of VC-4.

•If the VC-4 is filled by lower tributaries such as 34 Mbps, 2 Mbps or any of these two combinations, the AU pointer will not be filled by any information.

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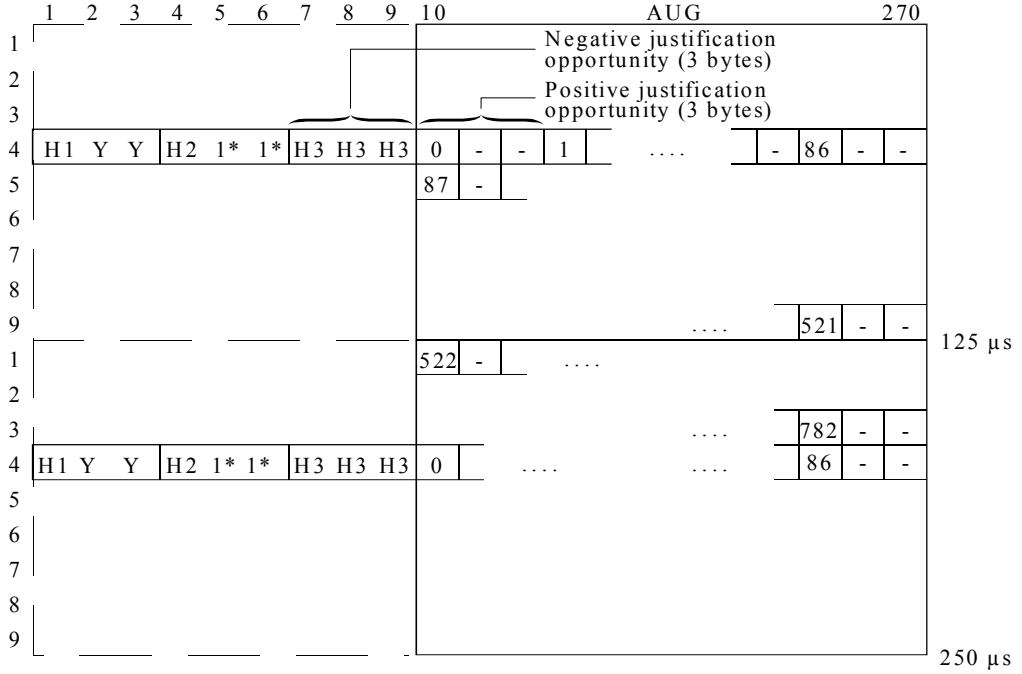
AU-4 Pointer offset numbering



• The AU-4 pointer value is a binary number with a range of 0 to 782 [to number (261 x 9)/3 bytes] which indicates the offset, in three-byte increments, between the pointer and the first byte of the VC-4 (POH is included in this numbering).
• Numbering starts from the first byte of the 4th row of VC.

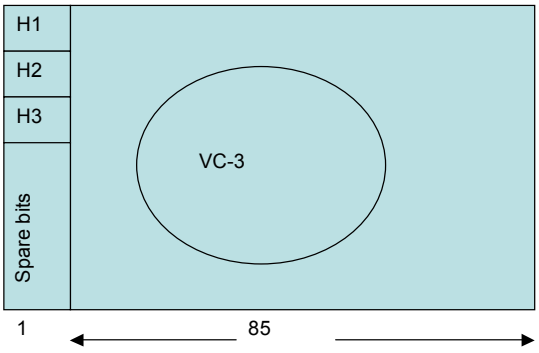
TU3 Pointer

Similar to AU pointer this TU3 pointer will be filled only when the VC-3 is filled directly from PDH 34 Mbps.

If it is filled by 2 Mbps these pointer bytes will be not be filled and will be treated as spare.

This points to VC-3 within the TU3 frame. Following shows TU3 pointer in the TU3 frame.

TU 4 pointer is similar to TU 3 pointer on its application.



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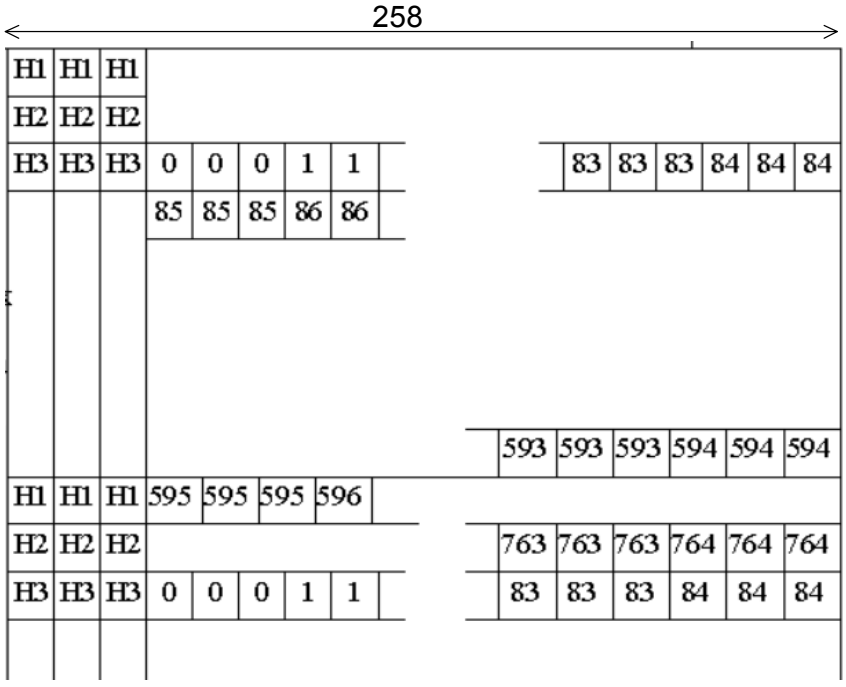
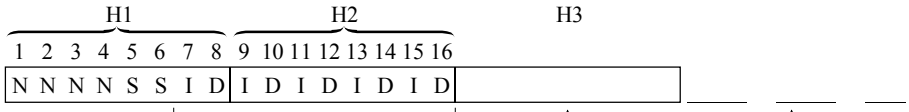
TU-3 Pointer offset numbering



The TU-3 pointer value is a binary number with a range of 0-764 [(255 x 9)/3] which indicates the offset between the pointer and the first byte of the VC-3 (POH is included).

AU-n/TU-3 Pointer (H1, H2, H3) Coding



I Increment
D Decrement
N New data flag

New data flag
– Enabled when at least 3 out of 4 bits match "1001"
– Disabled when at least 3 out of 4 bits match "0110"
– Invalid with other codes

Negative justification
– Invert 5 D-bits
– Accept majority vote

Pointer value (b7-b16)
– Normal range is:
for AU-4, AU-3: 0-782 decimal
for TU-3: 0-764 decimal

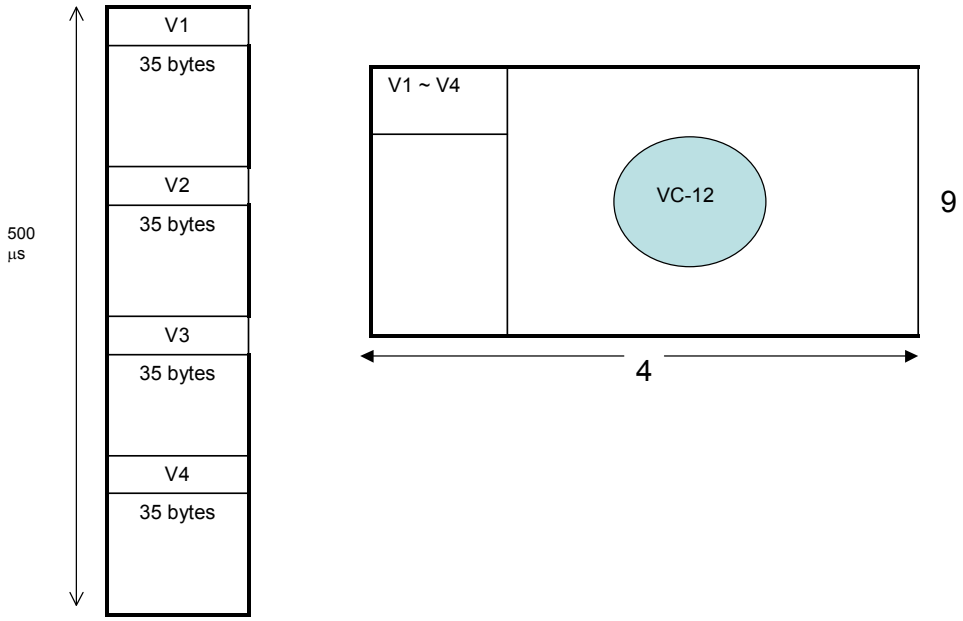
Positive justification
– Invert 5 I-bits
– Accept majority vote

Concatenation indication
– 1001SS1111111111 (SS bits are unspecified)

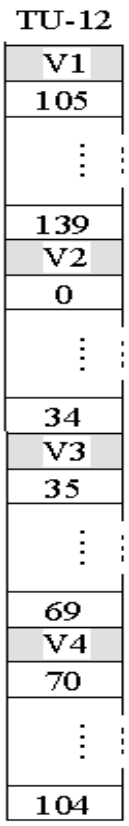
SS bits	AU-n/TU-n type
10	AU-4, AU-4-Xc, AU-3, TU-3

TU12 Pointer

This points to VC-12 within the TU12 frame. Following shows TU12 pointer in the TU12 frame.



TU-12 Pointer offset numbering



- The TU-12 pointer value contained in V1 and V2 indicates the offset from V2 (V3, V4 bytes are not counted) to the first byte of the VC-12.
- 0-139 which indicates the offset between the pointer and the first byte of the VC-12.
- That is, the value of the pointer for a TU-12 has a range of 0 to 140. For example, if the TU Payload Pointer has a value of 0, then the VC-12 begins in the byte adjacent to the V2 byte; if the TU Payload Pointer has a value of 35, then the VC-12 begins in the byte adjacent to the V3 byte.
- The V5 byte is the first byte of the VC-12 in the first multiframe.

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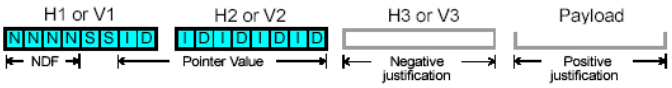
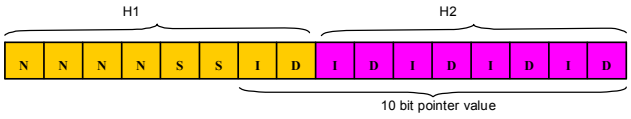
Details of the Pointer Coding



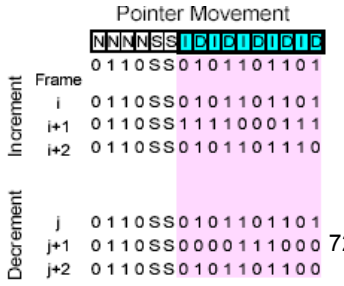
H1, H2 – Together are used to give the offset of the payload.



N- New Data Flag - Bits 1-4 (N-bits) of the pointer word carry an NDF. It is the mechanism which allows an arbitrary change of the value of a pointer. the normal value is "0110", and the value "1001" indicates a new alignment for the VC-n, and possibly new size. 1001 – enabled, 0110 – disabled

I – Increment bit, In positive justification 'I' bits are inverted
D – Decrement bit, In negative justification D bits are inverted.

SS – 10



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Operational Principles of a pointer

- H1 & H2 bytes : Indicates the offset value of the starting of a frame. Offset value can be of 3 types.
  - Offset zero – Zero justification : Frame starts in the normal word number 1.
  - Offset Positive – Positive Justification: Frame starts in the word number n. the value of n will be given in the H1 & H2 bytes.
  - Offset Negative - Negative Justification: Frame start in advance. Starting point will be one of the 9 bytes of the H3.

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Pointer Summary

Pointer		AU-4	TU-3	TU-12
		Provides a method of allowing flexible and dynamic alignment of the VC4 within the AU-4 frame.	Provides a method of allowing flexible and dynamic alignment of VC-3 within the TU-3 frame.	Provide a method of allowing flexible and dynamic alignment of the VC-12 the TU-multiframe
Location		Forth row (9 bytes) of Overhead byte section	Contained in TU-3 as three separate H1, H2 and H3 bytes	At the beginning of each frame (4 bytes - V1, V2, V3, V4.
H1, H2 (or V1, V2)		The pointer contained in H1 and H2 designates the location of the byte where the VC 4 begins.	The TU-3 pointer value contained in H1 and H2 designates the location of the byte where the VC-3 begins.	The TU-12 pointer value contained in V1 and V2 indicates the offset from V2 (V3, V4 bytes are not counted) to the first byte of the VC12
	N bits - Bits 1-4 of the pointer word	carry an NDF(New Data Flag) which allows an arbitrary change of the pointer value if that change is due to a change in the payload.	Carry an NDF which allows an arbitrary change of the value of the pointer if that change is due to a change in the VC-3.	Carry an NDF. It is the mechanism which allows an arbitrary change of the value of a pointer.
	SS bits - two S bits (bits 5 and 6)	Fixed - 01	Fixed - 01	Specify the size /indicate the Tributary Unit type. TU12 – 10
	I,D bits - The last ten bits (bits 7-16) of the pointer word	Carry the pointer value.	Carry the pointer value.	Carry the pointer value.
H3 / V3		Negative justification byte appears in the individual H3 byte of the AU-4 frame containing inverted D-bits. A positive justification byte appears immediately after the individual H3 byte of the AU-4 frame containing inverted I-bits	Negative justification byte appears in the individual H3 byte in the TU-3 frame containing inverted D-bits. A positive justification byte appears immediately after the individual H3 byte in the TU-3 frame containing inverted I-bits.	A positive justification opportunity immediately follows the V3 byte. Additionally, V3 serves as the negative justification opportunity such that when the opportunity is taken, V3 is overwritten by data
V4				Reserved
Pointer Value range		0 to 782 which indicates the offset, in three-byte increments, between the pointer and the first byte of the VC-4	0-764 which indicates the offset between the pointer and the first byte of the VC-3	0-139 which indicates the offset between the pointer and the first byte of the VC-12

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