

Synchronous Digital Hierarchy

SDH

Synchronous Digital Hierarchy (SDH)

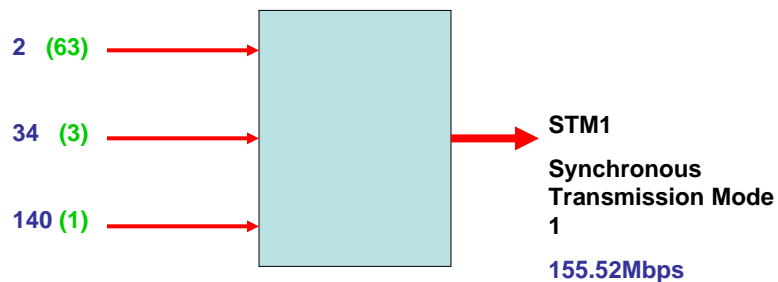
Synchronous Digital Hierarchy (SDH)	2
Plesiochronous Digital Hierarchy (PDH)	3
Synchronous Digital Hierarchy (SDH)	5
Principles	5
SDH structure	6
Accommodation of Bit Rates for SDH	12
Unification of Lower Tributaries of US & CEPT	13
Unification of Higher Tributaries of US & CEPT	14
Adaptation of STM in Satellites	16
Higher Order STM	16
Interface Between PDH and SDH	17
What is Justification	17
Formation of Tributary Units	19
Summary of Tributary Unit Formation	19
Path Overhead	20
Higher Order Path Overhead	20
Lower Order Path Overhead	27
Pointers	30
Functions of a Pointer	31
Operational Principles of a pointer	37
Pointer Summary	37
SDH Major Operational Components	38
Summary of SDH Management Sections	38
Regenerator Section Overhead	39
Multiplex Section Overhead	40
Summary of SDH Mapping, Aligning, Pointer processing & Multiplexing	42
Examples of SDH Networks	46
Examples of Local SDH Network	46
Examples of Global SDH Network	47

Synchronous Digital Hierarchy (SDH)

- Characteristics
 - Can combine European & American PDH
 - Basically based on Synchronous Optical Network – SONET (American)
 - The following PDH (European) can be multiplexed

3

Multiplexing of PDH Tributaries to STM1



4

Various Combinations of PDH Tributaries to STM1

- 2.048 Mbps (63 channels) or 34 Mbps (3 channels) or 140 Mbps (1 channel) will form an STM1.
- n_1 of 2.048 Mbps, n_2 of 34 Mbps can be multiplexed where n_1 & n_2 will give rise to a total of less than 155.52 Mbps;
 - if $n_2 = 2$, $n_{1(max)} = 21$
 - $n_2 = 1$, $n_{1(max)} = 42$

5

Plesiochronous Digital Hierarchy (PDH) - Principles

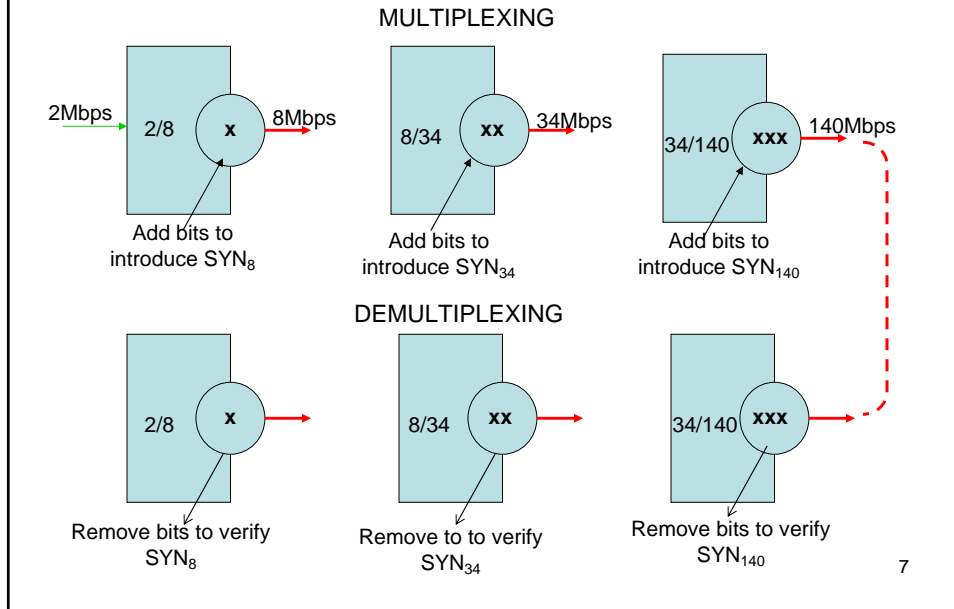
- Basic bit period shrunk at each point from 2 Mbps upwards (multiplexing) and at each multiplexing point bits are added.

Example:

<u>Speed</u>	<u>Bit Period</u>	<u>Added bits (assume)</u>
2 Mbps	488 ns	
8 Mbps	118 ns	X
34 Mbps	25 ns	X ₁
140 Mbps	7 ns	X ₂
560 Mbps	1.7 ns	X ₃

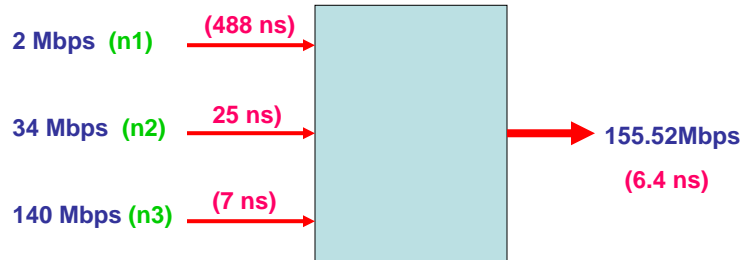
6

The Principles of PDH



- At each de-multiplexing point bit period expands, and the inserted bits are removed
- Hence from example, 560 Mbps stream, an 8 Mbps stream cannot be obtained direct. 560 Mbps has to be converted to 140 Mbps, then to 34 Mbps, and then to 8 Mbps; due to the extraction of overhead bits at each de-multiplexing point.
- PDH means Plesiochronous digital Hierarchy. Plesiochronous means Multiple synchronization. That is why the above cannot be achieved.

Synchronous Digital Hierarchy (SDH) - Principles



9

- Different periods of bits are multiplexed to form a single period of 6.4 ns
- Similarly, from 6.4 ns different periods can be obtained at de-multiplexing points
- All treatment will be done at the entrance from 2 Mbps, 34 Mbps or 140 Mbps into STM1
- No additional bits are introduced within STM1 (after entrance) transforming from 2 Mbps or 34 Mbps or 140 Mbps to STM1

10

PDH to SDH at the Entry

- SDH is always of higher frequency than PDH. The treatment to the deviation of the PDH streams has to be accommodated in the SDH stream. Complexity increases when the higher order PDH stream to be placed in the SDH stream. Hence positive, negative & zero justification to be applied, depending upon the PDH stream at the entry to SDH.
- Management of PDH tributary (bit stream) throughout SDH and back again to de-multiplex to PDH
- This management information is called 'path Overhead' (POH). Exchange at which this tributary to be terminated, error control etc.
- At the entry to SDH stream, any PDH tributary will be treated for positive, negative & zero justification, depending upon the primary PCMs characteristics. POH and stuffing bits to convert to a single bit period of 6.4 ns. After this no additional bits are introduced to further shrink the period of 6.4 ns.
- Even in higher order SDH, assume STM4, no additional bits introduced. In STM4 the bit period exactly $(6.4 \text{ ns})/4 = 1.6 \text{ ns}$
- Same concept extends for higher order STM.

11


SDH structure

- Basic Structure
 - In 125 μs , 2430 words, each word represent 8 bits which is equivalent to a sample. Hence for 1 second there are 155.52 Mb.
 - Uses word (byte) interleaving. Hence easy to manage.
 - In order to analyze the structure these 2430 words are organized in 9 rows with 270 columns as follows:

12

Basic Structure

1	1	2		270
2	271			
3				
4				
5				
6				
7				
8				2160
9	2161			2430



 $125 \mu\text{s}$

$125 \mu\text{s} \rightarrow 2430 \times 8 \text{ bits}$

$1 \mu\text{s} \rightarrow 155.52 \text{ Mbits}$

13

Structure for 2 Mbps and 34 Mbps

2.048 Mbps

1	1	2	3	4
2	5
3
4
5
6
7
8	32
9	33	34	35	36

$125 \mu\text{s} \Rightarrow 36 \times 8$

$1\text{s} \Rightarrow 2304 \text{ kb}$

Spare bits = 0.256 (12.5%)

Spare bits = Path Overhead + justification

34.368 Mbps

1	2	83	84
85
..
..
..
..
..
..
..	755	756

$125 \mu\text{s} \Rightarrow 756 \times 8$

$1\text{s} \Rightarrow 48.384 \text{ kb}$

Spare bits = 14.02 (40%)

Further reviewed on slide # 15

For 34 Mbps structure 21 Nos. 2.048 Mbps can be placed

14

Observations

- For 34 Mbps in PDH 2.048 Mbps, 16 streams can be multiplexed
- In SDH 21 Nos. can be multiplexed, WHY?
- For PDH, CEPT 34.368 Mbps and PDH American equipment is 44.736 Mbps, Hence 84 columns are used for 44.736 Mbps American system, SDH stream stems from American SONET.
(CEPT – Committee of European Post & Telecommunication)
- Hence it has been designated for American 44.736 Mbps, though we are using it for CEPT 34Mbps. That's why there are many spare bits if we use it for 34Mbps directly on STM1.

15

Structure of 34 Mbps when formed from 2Mbps

(Actual 34.368Mbps)

1	1	2	83	84
2	85
3
4
5
6
7
8
9	755	756
	1	2	84

For 125 μ s => 756 x 8 bits

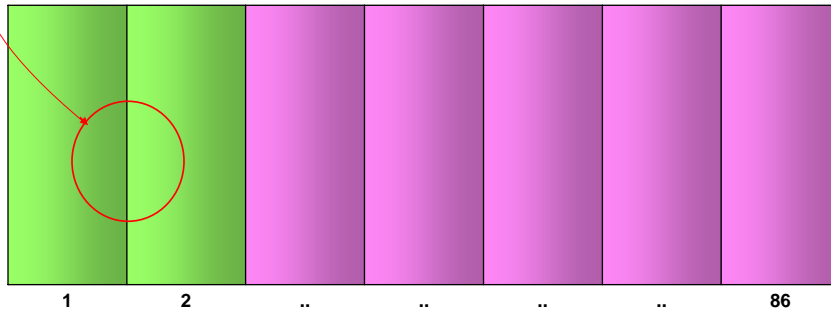
1 s => 48384

Spare bits for POH + Justification= 9.3444 (6.7%)

16

Structure of 34Mbps in STM1 when formed from 34 Mbps itself

- Every basic tributary has to accommodate for each POH + Justification
- Hence for 34 direct to be placed, it needs two more columns to accommodate POH + Justification



If we fill with 21 Nos. of 2.048 Mbps, these first two columns are spare

17

Structure of 140 Mbps in STM1 when formed from 34Mbps

(Actual 139.264 Mbps)

1	1	2	257	258
2	259
3
4
5
6
7
8	1464
9	1465	2321	2322
	1	2	258

For 125 μ s \Rightarrow 2322 x 8 bits

1 s \Rightarrow 148.605

Spare bits for POH + Justification = 9.3444 (6.7%)

18

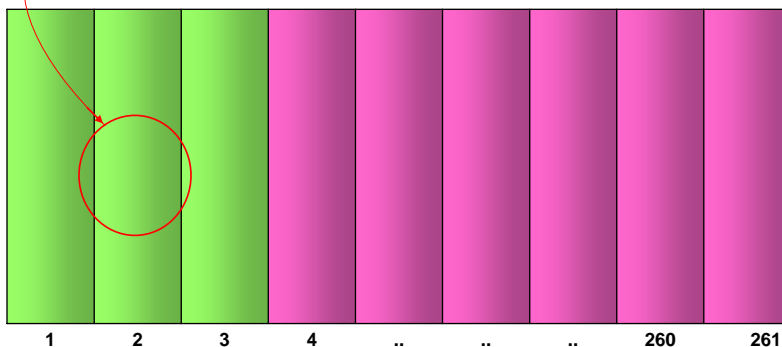
Observations

- For 140 Mbps is PDH (CEPT) there are 4 Nos. 34 Mbps streams. But in SDH only 3 Nos 34 Mbps can be accommodated
- 63 Nos 2.048 Mbps can be accommodated in SDH.
- No equipment for PDH 140 Mbps (America)

19

Structure of 140Mbps in STM1 when formed from 140Mbps itself

- Similar reasoning as for 34 Mbps, in order to direct 140 Mbps into SDH, One might think that 3 columns are used for POH and Justification, but it is not. Why?



If we fill with 3 of 34 Mbps, these first 3 columns are spare

20

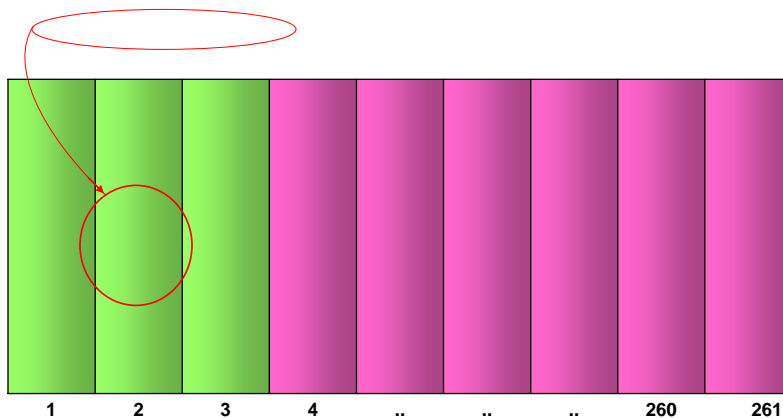
Bytes Allocated for Justification and Matching the speed variations input tributaries

- When we consider TU12, 12.5% bits are available for matching the variations as well as for justification.
- For similar variations TU3 40.0% bits are available
- But or similar variations in TU4, if we use 258 columns 6.7% bits are available, which is not enough when we consider the bit speed. Hence 2 more columns are kept for the treatment of variations in 140Mbps as well as justification (to be adjusted). Hence there is a deviation from the previous thinking and 260 columns are allocated for 140 Mbps instead of 258 columns. One more column is allocated for POH and for the Pointer first 9 bytes of the 4th Row is allocated.

21

Structure of 140Mbps in STM1 when formed from 140Mbps itself

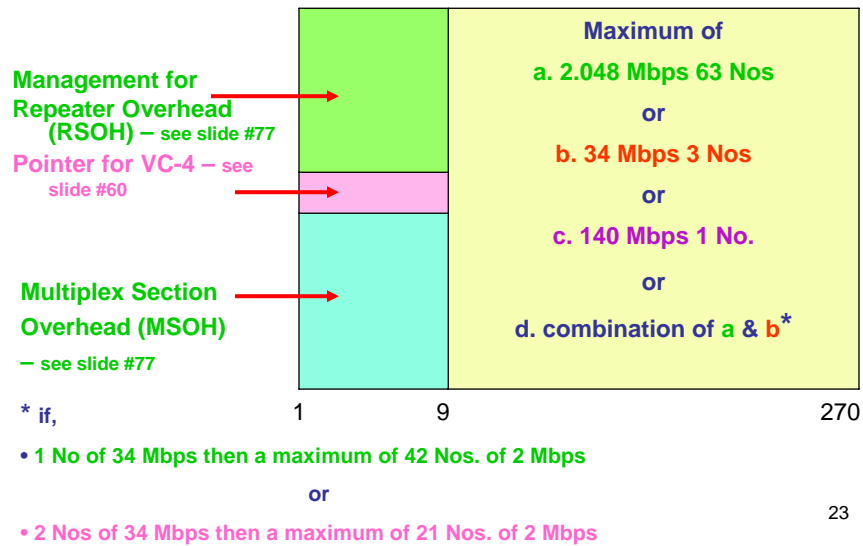
- Additional 3 columns are



If we fill with 3 of 34 Mbps, these first 3 columns are spare

22

Accommodation of Bit Rates for SDH



Building blocks of STM1

- 2 Mbps is the lowest speed for European system to be connected to STM1
- Then 34 Mbps and 140 Mbps systems can be connected
- 8 Mbps cannot be connected to STM1
- STM1 can be made either from 140 Mbps or a combination of 2Mbps and 34 Mbps. Hence the basic building block has been designed to accommodate the above thinking
- TU is the basic building block of SDH, from PDH for 2 Mbps or 34 Mbps
 - TU12 = 2 Mbps
 - TU3 = 34 Mbps
- Intermediate multiplexing point has been created to accommodate American systems.

24

PDH

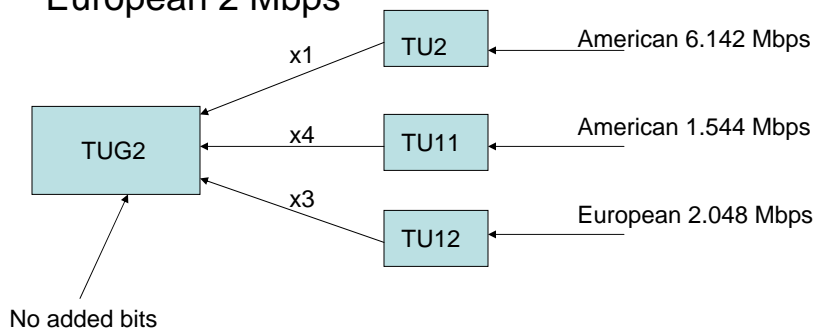
There are 3 standards in the world: CEPT, North America and Japan. SDH can combine all these 3 systems except CEPT 8.448Mbps and Japan 32.064Mbps and 97.728 Mbps

* - these bit rates are not directly accommodated in SDH

CEPT Mbps	North America Mbps	Japan Mbps
2.048	1.544	1.544
8.448*	6.312	6.312
34.368	44.376	32.064*
139.264		97.728*

Unification of Lower Tributaries of US & CEPT

- For example, TUG2 to accommodate American 6 Mbps and 1.5 Mbps with European 2 Mbps

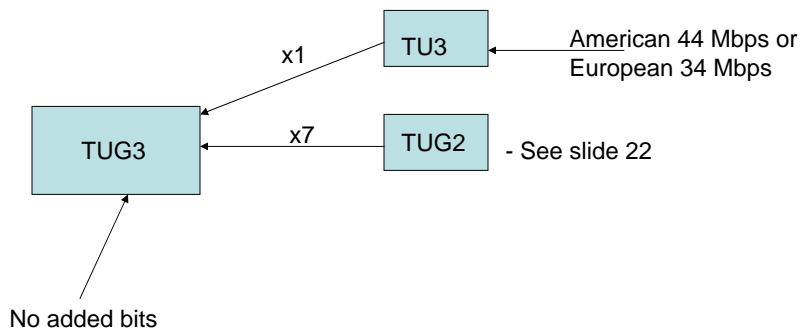


26

- Also intermediate multiplexing point has been introduced in addition to mixing of European and American systems to accommodate lower speed tributaries
- Ex: TUG3
- While TUG3 can accommodate European 34 Mbps and American 44Mbps, it can accommodate 7 of TUG 2
- See next slide

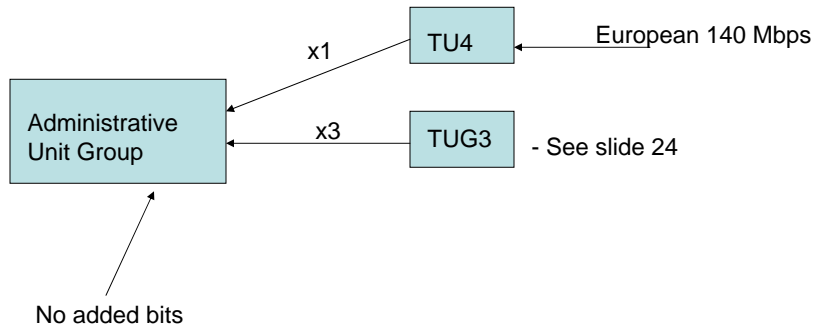
27

Unification of Higher Tributaries of US & CEPT



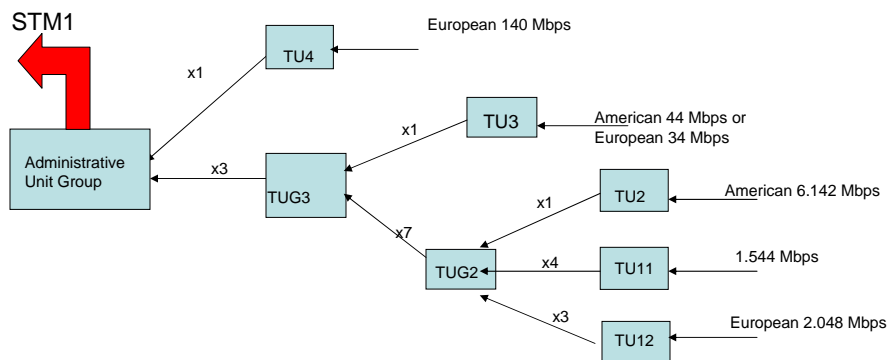
28

- Highest multiplexing point has been introduced to accommodate European 140 Mbps and to accommodate lower bit speed tributaries



29

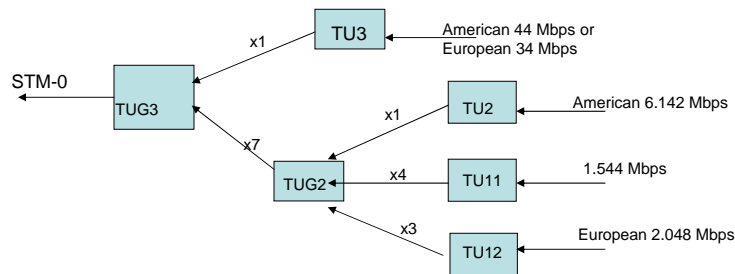
Summary of Multiplexing up to STM1



30

Adaptation of STM in Satellites

- Instead of 155.52 Mbps a lower bit rate 51.84 Mbps is adopted for satellite communication.



31

Higher Order STM

- Unlike PDH, in SDH when it goes to higher order no additional bits are inserted at higher order multiplexing points. The following gives the details of higher order STMs.

	Bit rate (Mbps)	Approximate bit rates	Calculation of higher order bit rates	No. of voice channels	Bit period
STM1	155.52			1,890	6.4ns
STM4	622.08		=155.52 x 4	7,560	1.6ns
STM16	2488.32	~2.5Gbps	=622.08 x 4	30,240	400ps
STM64	9953.28	~10Gbps	=2488.32 x 4	120,960	100ps

Note: Conventional CEPT PCM of 30 channels is assumed.

32

Interface Between PDH and SDH

- For explanation CEPT system is used. Same concept applies for other systems.
- PDH tributary will be converted to a virtual container by adding Path Overhead (POH) bits, so that each tributary the originating and destination nodes can be identified.
- This Virtual Container (VC) will be added a Pointer. Hence, made as a Tributary Unit (TU). The pointer thus added will provide the justification of PDH tributary with respect to the SDH tributary.
- The pointer will help at the demultiplexing point to demultiplex to the correct phase of the original PDH signal.

33

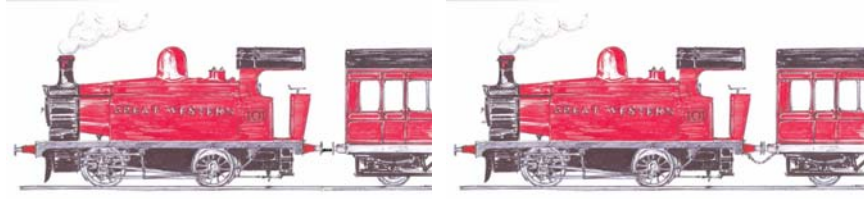
What is Justification

- Imagine 2 compartments of a train. It is connected with a pair of buffers and flexible chain.
- If the first moving compartment going faster the next. The chain will pull the next compartment. This is equivalent to 'Positive Justification.'
- If the first compartment is moving slower than the next the buffers will collide and slow down the next one. This is equivalent to 'Negative Justification'.
- In this example, the first moving compartment is analogous to higher order tributary and the next is equivalent to primary tributary.

34

Train Analogy

Buffer – chain coupling mechanism



- Positive Justification
- Tension in the chain
- Negative Justification
- Compression in the buffer

35

Effects of Justification

- Assume secondary tributary speed f_s
- Assume primary tributary speed f_p
- If $f_s > f_p$, Positive Justification, the effect will be to read one information bit of primary as two information bits of secondary. Hence, in secondary one bit has to be inhibited.
- If $f_s < f_p$, Negative Justification, the effect will be to lose one information bit of primary in the secondary. Hence, in secondary one bit has to be introduced.
- If $f_s = f_p$, Zero Justification, the ideal situation but difficult to realize in practice.
- In SDH, all the above 3 justifications will be achieved by introduction of a pointer in addition to the information and path overhead bits.

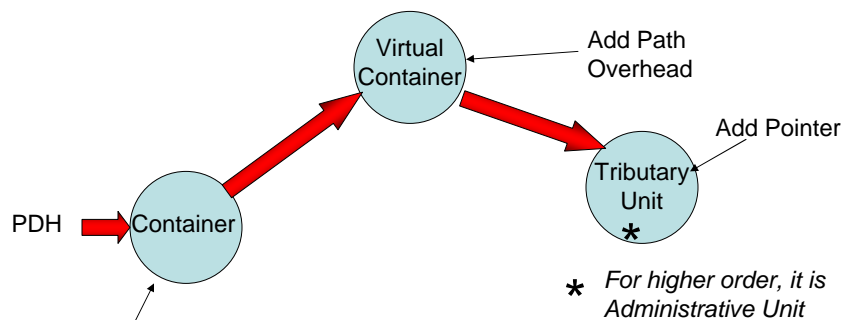
36

Formation of Tributary Units

- In SDH, the basic PDH tributary (whether 2Mbps, 34Mbps or 140Mbps) will be carried in any order of STM as a respective tributary unit of TU-12, TU-3 or AU-4.
- The basic PDH will be treated at the entrance as a container of bits. This container will be added certain overhead bits to match to the STM bit period of 6.7ns. This is called a container (C-12, C-3 or C-4).
- These containers are then added with management-bits-like path overhead. POH plays vital role in operation, administration and maintenance of original PDH tributaries up to the transportation to the required destination of the same. The basic functions of POH includes error detection and transmission path verification. So that this container can be treated as a Virtual Container (VC). Hence this will become VC-12, VC-3 or VC-4.
- This virtual container will be further added with Justification Bits or called as a Pointer to indicated the phase differences between the PDH tributaries with respect to the STM1.
- The STM1 will have a separate pointer to be used when it is multiplexed further to a higher order SDH.

37

Summary of Tributary Unit Formation



Let's study:

1. Path Overhead
2. Pointer

38

Higher Order Path Overhead

There are 9 words for POH, which are listed below:

J1	Path trace - connection verification
B3	Path bit interleaved parity (BIP-8) - parity computed over previous container
C2	Path signal label - mapping type in VC-n
G1	Path status - monitoring of bidirectional path status
F2	Path user channel - 64 kbit/s user channel for operators
H4	Tributary unit multiframe indicator - start of multiframe
F3	Path user channel - 64 kbit/s user channel for operators
K3	Automatic Protection Switching (APS) - path protection
N1	Network operator byte - higher order tandem connection overhead (TCOH)

39

Details of J1 & B3 of Higher Order POH

- **J1 - Higher-Order VC-N path trace byte**
This user-programmable byte repetitively transmits a 15-byte string plus 1-byte CRC-7. A 64-byte free-format string is also permitted for this Access Point Identifier. This allows the receiving terminal in a path to verify its continued connection to the intended transmitting terminal.
- **B3 - Path Bit Interleaved Parity code (Path BIP-8) byte**
This is an even-parity code, used to determine if a transmission error has occurred over a path. Its value is calculated over all the bits of the previous virtual container before scrambling and placed in the B3 byte of the current frame. (BIP-8 is calculated on the 8 bit blocks of the n^{th} frame and placed on the $(n+1)^{\text{th}}$ frame of VC3/VC4.)

40

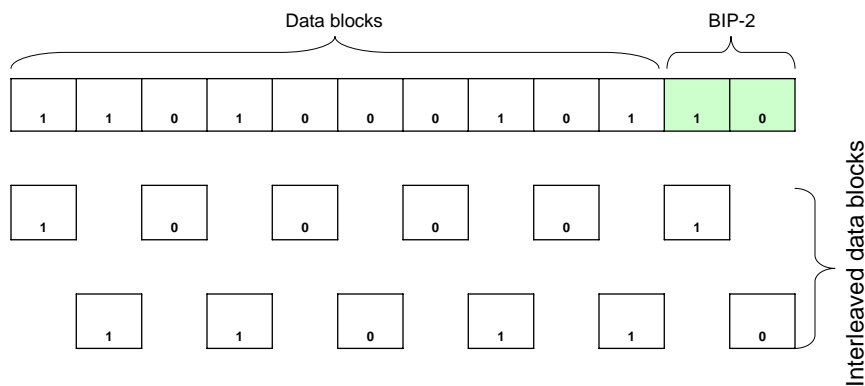
What is BIP?

- Bit Interleaved Parity
- Error monitoring in SDH uses a CRC with a polynomial, x^n+x^0 , called Bit Interleaved Parity (BIP-n).
- The signal to be monitored is divided in to small blocks with n-bit size. The even parity check is applied to each bit of all the blocks in the signal, from m 1st to nth bit independently.

41

Example of BIP

- The following is an illustration of BIP-2 on a bit stream of 10 information bits and 2 even parity bits.



42

Application of BIP in SDH Systems

Following table gives the varying values of n used at different stages of the multiplexing of an SDH signal

Frame	Order of BIP (n)	Reference abbreviation to the Overhead Byte
RSOH	BIP-8	B1
MSOH	BIP-24	B2
VC-4	BIP-8	B3
VC-3	BIP-8	B3
VC-12	BIP-2	V5 (b1,b2)

43

Details of C2 of Higher Order POH

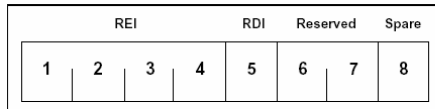
- **C2 - Path signal label byte** – This byte specifies whether the virtual container is equipped or not and the mapping type in the respective virtual container. Standard binary values for C2 are:

MSB	LSB	Hex Code	Interpretation
Bits 1-4	Bits	5-8	
0000	0000	00	Unequipped or supervisory-unequipped
0000	0001	01	Equipped – non-specific
0000	0010	02	TUG structure
0000	0011	03	Locked TU-n
0000	0100	04	Asynchronous mapping of 34,368 kbit/s or 44,736 kbit/s into the Container-3
0001	0010	12	Asynchronous mapping of 139,264 kbit/s into the Container-4
0001	0011	13	ATM mapping
0001	0100	14	MAN DQDB (IEEE Standard 802.6) mapping
0001	0101	15	FDDI (ISO Standard 9314) mapping
0001	0110	16	Mapping of HDLC/PPP (Internet Standard 51) framed signal
0001	0111	17	Mapping of Simple Data Link (SDL) with SDH self synchronising scrambler
0001	1000	18	Mapping of HDLC/LAP-S framed signals
0001	1001	19	Mapping of Simple Data Link (SDL) with set-reset scrambler
0001	1010	1A	Mapping of 10 Gbit/s Ethernet frames (IEEE 802.3)
1100	1111	CF	Obsolete mapping of HDLC/PPP framed signal
1110	0001	E1	Reserved for national use
:	:	:	:
1111	1100	FC	Reserved for national use
1111	1110	FE	Test signal, 0.181 specific mapping
1111	1111	FF	VC-AIS

14

Details of G1 of Higher Order POH

- **G1 - Path status byte** – This byte is used to convey the path terminating status and performance back to the originating path terminating equipment. Therefore the bi-directional path in its entirety can be monitored, from either end of the path.



Byte G1 is allocated to convey back to a VC-4-Xc/VC-4/VC-3 trail termination source the status and performance of the complete trail. Bits 5 to 7 may be used to provide an enhanced remote defect indication with additional differentiation between the payload defect (PLM), server defects (AIS, LOP) and connectivity defects (TIM, UNEQ). The following codes are used:

<u>Bits 5-7</u>	<u>Meaning</u>	<u>Triggers</u>	
001	No remote defect	No remote defect	REI – Remote Error Indicator (for path) An indication returned to a transmitting node (source) that an errored block has been detected at the receiving node (sink). REI was previously known as Far End Block Error (FEBE). RDI – Remote Defect Indicator (for terminal)
010	E-RDI Payload defect	PLM	
101	E-RDI Server defect	AIS, LOP	
110	E-RDI Connectivity defect	TIM, UNEQ	

45

Details of G1 of Higher Order POH

(contd.)

- The E-RDI G1 (bits 5-7) code interpretation provides for interworking with equipment which supports RDI. It is not necessary for the interpretation to identify if the equipment supports RDI or E-RDI. For the E-RDI codes, bit 7 is set to the inverse of bit 6. Following is the E-RDI G1 (bits 5-7) code interpretation:

<u>Bits 5-7</u>	<u>E-RDI Interpretation</u>
000	No remote defect (Note 1)
001	No remote defect
010	E-RDI Payload defect (Note 2)
011	No remote defect (Note 1)
100	E-RDI Server defect (Note 1)
101	Remote E-RDI Server defect
110	Remote E-RDI Connectivity defect
111	Remote E-RDI Server Defect (Note 1)

NOTE 1: These codes are generated by RDI supporting equipment and are interpreted by E-RDI supporting equipment as shown. For equipment supporting RDI, clause 9.3.1.4/G.707, this code is triggered by the presence or absence of one of the following defects: AIS, LOP, TIM, or UNEQ. Equipment conforming to an earlier version of this standard may include PLM as a trigger condition. ATM equipment complying with the 1993 version of ITU-T Recommendation I.432 may include LCD as a trigger condition. Note that for some national networks, this code was triggered only by an AIS or LOP defect.

NOTE 2: ATM equipment complying with the 08/96 version of ITU-T Recommendation I.432.2 may include LCD as a trigger condition.

46

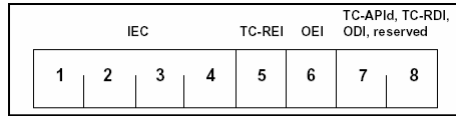
Details of F2, H4, F3 & K3 of Higher Order POH

- F2 – Path user channel byte – This byte is used for user communication between path elements.
- H4 – Position and Sequence Indicator byte – This byte provides a multi frame and sequence indicator for virtual VC-3/4 concatenation and a generalized position indicator for payloads. In the latter case, the content is payload specific (e.g., H4 can be used as a multiframe indicator for VC-2/1 payload). For mapping of DQDB in VC-4, the H4 byte carries the slot boundary information and the Link Status Signal (LSS). Bits 1-2 are used for the LSS code as described in IEEE Standard 802.6. Bits 3-8 form the slot offset indicator. The slot offset indicator contains a binary number indicating the offset in octets between the H4 octet and the first slot boundary following the H4 octet. The valid range of the slot offset indicator value is 0 to 52. A received value of 53 to 63 corresponds to an error condition.
- F3 - Path user channel byte – This byte is allocated for communication purposes between path elements and is payload dependent.
- K3 - APS signalling is provided in K3 bits 1-4, allocated for protection at the VC-4/3 path levels. K3 bits 5-8 are allocated for future use. These bits have no defined value. The receiver is required to ignore their content. ⁴⁷

Details of N1 of Higher Order POH

- N1 - Network operator byte – This byte is allocated to provide a Higher-Order Tandem Connection Monitoring (HO-TCM) function. N1 is allocated for Tandem Connection Monitoring for contiguous concatenated VC-4, the VC-4 and VC-3 levels.

Details of N1 of Higher Order POH (contd.)



Bits 1-4	Incoming Error Count (IEC).
1001	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1110	Incoming AIS

NOTE: To guarantee a non all-zeroes N1 byte independent of the incoming signal status, it is required that the IEC code field contains at least one "1". When zero errors in the BIP-8 of the incoming signal are detected, an IEC code is inserted with "1"s in it. In this manner, it is possible for the Tandem Connection sink at the tail end of the Tandem Connection link to use the IEC code field to distinguish between unequipped conditions started within or before the Tandem Connection.

49

Details of N1 of Higher Order POH (contd.)

- Bit 5 - Operates as the TC-REI of the Tandem Connection to indicate errored blocks caused within the Tandem Connection.
- Bit 6 - Operates as the OEI to indicate errored blocks of the egressing VC-n.
- Bit 7,8 - Operate in a 76 multiframe as:
 - Access point identifier of the Tandem Connection (TC-APId); it complies with the generic 16-byte string format given in 9.2.2.2.
 - TC-RDI, indicating to the far end that defects have been detected within the Tandem Connection at the near end Tandem Connection sink.
 - ODI, indicating to the far end that AU/TU-AIS has been inserted into the egressing AU-n/TU-n at the TC-sink due to defects before or within the Tandem Connection.
 - Reserved capacity (for future standardization).

50

Details of N1 of Higher Order POH (contd.)

Frame #	Bits 7-8 definition	
1-8	Frame Alignment Signal: 1111 1111 1111 1110	
9-12	TC-APId byte #1 [1 C ₁ C ₂ C ₃ C ₄ C ₅ C ₆ C ₇]	
13-16	TC-APId byte #2 [0 X X X X X X X]	
17-20	TC-APId byte #3 [0 X X X X X X X]	
:	:	
65-68	TC-APId byte #15 [0 X X X X X X X]	
69-72	TC-APId byte #16 [0 X X X X X X X]	
73-76	TC-RDI, ODI and Reserved (see following)	
Frame #	Bit 7 definition	Bit 8 definition
73	Reserved (default = "0")	TC-RDI
74	ODI	Reserved (default = "0")
75	Reserved (default = "0")	Reserved (default = "0")
76	Reserved (default = "0")	Reserved (default = "0")

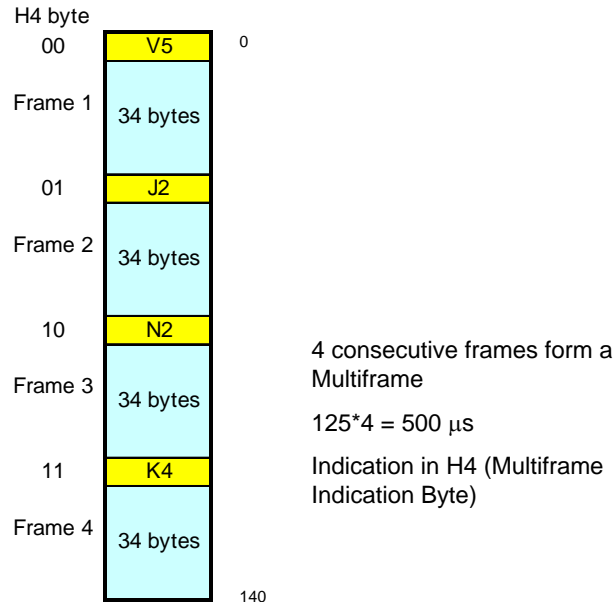
51

Structure of TU12

The structure of TU3 is such that in a given 125 μ s frame when mapped directly from 34Mbps to VC3 and then to TU3 there are enough spare words to accommodate the POH and Pointer. However in the case of 2Mbps the number of spare words to accommodate POH and Pointer in a given 125 μ s period is not sufficient enough. Hence 4 frames of 125 μ s are used to indicate the POH and Pointer for the respective 2Mbps PDH stream. The slide shows how the POH is accommodated for 2Mbps tributary streams:

52

The Structure of VC12 POH



53

Details of V5 of Lower Order POH

- V5 – VT path overhead

BIP-2		REI	RFI	Signal Label			RDI
1	2	3	4	5	6	7	8

- Bits 1-2 Allocated for error performance monitoring. A Bit Interleaved Parity (BIP-2) scheme is specified. Includes POH bytes, but excludes V1, V2, V3, and V4.
- Bit 3 A VC-2/VC-1 path Remote Error Indication (LP-REI) that is set to one and sent back towards a VC-2/VC-1 path originator if one or more errors were detected by the BIP-2; otherwise set to zero.
- Bit 4 A VC-2/VC-1 path Remote Failure Indication (LP-RFI). This bit is set to one if a failure is declared, otherwise it is set to zero. A failure is a defect that persists beyond the maximum time allocated to the transmission system protection mechanisms.
- Bits 5-7 Provide a VC-2/VC-1 signal label. The Virtual Container path Signal Label coding is:
- 000 Unequipped or supervisory-unequipped
 - 001 Equipped – non-specific
 - 010 Asynchronous
 - 011 Bit synchronous
 - 100 Byte synchronous
 - 101 Reserved for future use
 - 110 Test signal, 0.181 specific mapping
 - 111 VC-AIS
- Bit 8 Set to 1 to indicate a VC-2/VC-1 path Remote Defect Indication (LP-RDI); otherwise set to zero.

54

Details of J2 of Lower Order POH

- J2 - Used to repetitively transmit a Lower-Order Access Path Identifier so that a path receiving terminal can verify its continued connection to the intended transmitter. A 16-byte frame is defined for the transmission of Path Access Point Identifiers. This 16-byte frame is identical to the 16-byte frame of the J1 and J0 bytes.

55

Details of N2 of Lower Order POH

(contd.)

- N2 - Allocated for Tandem Connection Monitoring for the VC2, VC-12, and VC-11 level.

BIP-2		Incoming "1"			TC-APId, TC-RDI, ODI, reserved		
b1	b2	AIS	TC-REI	OEI	b7	b8	
b1	b2	b3	b4	b5	b6	b7	b8

- Bits 1-2 Used as an even BIP-2 for the Tandem Connection.
- Bit 3 Fixed to "1". This guarantees that the contents of N2 is not all zeroes at the TC- source. This enables the detection of an unequipped or supervisory unequipped signal at the Tandem Connection sink without the need of monitoring further OH-bytes.
- Bit 4 Operates as an "incoming AIS" indicator.
- Bit 5 Operates as the TC-REI of the Tandem Connection to indicate errored blocks caused within the Tandem Connection.
- Bit 6 Operates as the OEI to indicate errored blocks of the egressing VC-n.
- Bits 7-8 Operate in a 76 multiframe as:
- The access point identifier of the Tandem Connection (TC-APId)
 - The TC-RDI, indicating to the far end that defects have been detected within the Tandem Connection at the near end Tandem Connection sink.
 - The ODI, indicating to the far end that TU-AIS has been inserted at the TC-sink into the egressing TU-n due to defects before or within the Tandem Connection.
 - Reserved capacity (for future standardization).

56

Details of N2 of Lower Order POH (contd.)

Frame #	Bits 7-8 definition
1-8	Frame Alignment Signal: 1111 1111 1111 1110
9-12	TC-APId byte #1 [1 C ₁ C ₂ C ₃ C ₄ C ₅ C ₆ C ₇]
13-16	TC-APId byte #2 [0 X X X X X X X]
17-20	TC-APId byte #3 [0 X X X X X X X]
:	:
65-68	TC-APId byte #15 [0 X X X X X X X]
69-72	TC-APId byte #16 [0 X X X X X X X]
73-76	TC-RDI, ODI and Reserved (see following)

Frame #	Bit 7 definition	Bit 8 definition
73	Reserved (default = "0")	TC-RDI
74	ODI	Reserved (default = "0")
75	Reserved (default = "0")	Reserved (default = "0")
76	Reserved (default = "0")	Reserved (default = "0")

57

Details of K4 of Lower Order POH

- K4 - Bits 1-4 are allocated for APS signalling for protection at the Lower-Order path level. Bits 5-7 are reserved for optional use. Bit 8 is reserved for future use and has no defined value.

58

Comparison of POH in Higher and Lower Orders

Function	VC3,4 POH Byte	VC12 POH Byte
verification of VC connection	J1	J2
Bit Interleaved parity Check Byte	B3	V5(b1-b2)
Indication of VC composition	C2	V5(b5-b7)
Remote Alarm Indication	G1	V5(b3,4,8)
64kb clear channels	F2,F3	N/A
Multiframe Position Indicator	H4	N/A
Automatic Protection Switch signaling	K3	K4
Network Operator Byte	N1	N2
Spare (unused)		

59

Pointers

- Application of Pointer

- A Pointer is used to address a particular location within an AU or a TU structure. There are mainly 2 types of pointers

1. AU Pointers: used to point at Higher Order VC's (VC-4,3) in an STM frame
2. TU Pointers: used to point at Lower Order VC's (VC-12) in higher order VC

Each of these pointers carry the offset number (address) at which the 1st byte of the payload is located, within the frame. The offset numbering of AU4, TU3, TU12, frames are shown in slide # 66, 68, 71. The offset numbering of TUs/AUs will be according to the CCITT Rec. G.707.

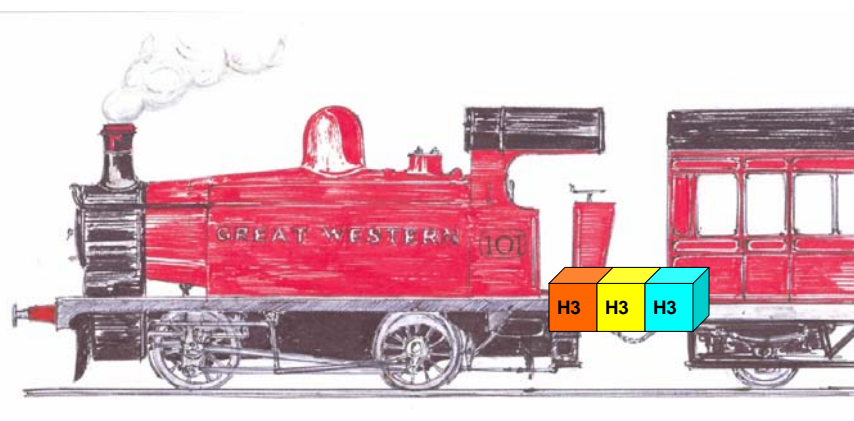
60

Functions of a Pointer

- 1. Minimization of multiplexing Delay
 - This is the main advantage of pointers. Normally signals from different originating points differ in their phases, because of different transmission length and different clock generation. In the usual multiplexing process, to align them, each signal has to be written into memories and read out using a new phase of the frame to be multiplexed. Thus, it is inevitable to cause additional delay of half of the frame time in average and one frame time at maximum. Also, it requires large capacity memories.
 - To avoid above inconveniences, this pointer method was introduced into the multiplexing of SDH signal. A pointer is assigned to each VC to be multiplexed and it indicates relative phase shift between the VC and the new frame by using the address number in the new frame. As a matter of course, every VC has different pointer value. The pointer is renewed at every multiplexing process, so it is not necessary to introduce undesirable additional delays.
- 2. Frequency Justification
 - Generally this function is not required in an SDH network since all network elements are synchronized to a single clock. But if the VC's are transported over different networks, and if a network element is in an abnormal condition, justification is necessary to absorb any frequency differences between payload and the frames. There are 2 types of justification in SDH:
 - a. Positive Justification: If the frame speed of the STM is higher than the payload arrival speed.
 - b. Negative justification: If the frame speed of the STM is lower than the payload arrival speed.

61

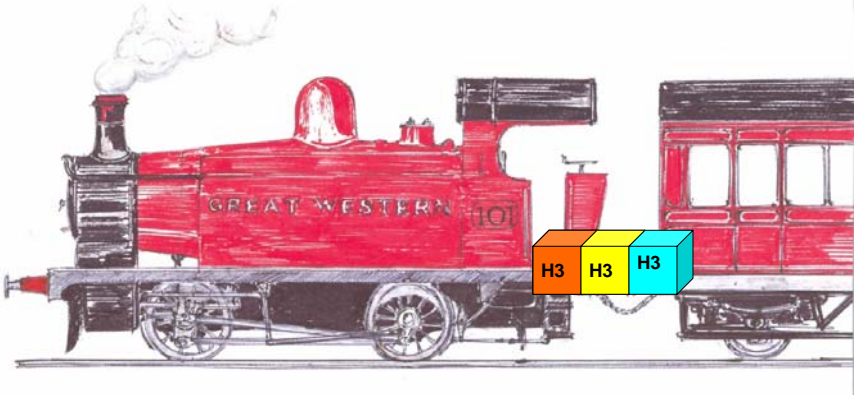
Positive justification



Application of the chain in the Train analogy.

62

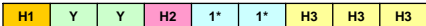
Negative justification



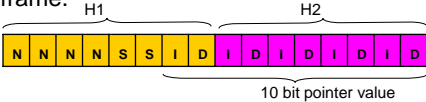
Application of the buffer in the Train analogy.

AU-4 Pointer

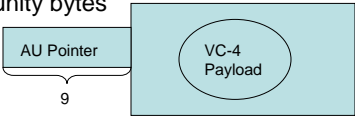
- This pointer points to the VC-4 in an STM-1 frame. Following is the typical structure of an AU-4 pointer.



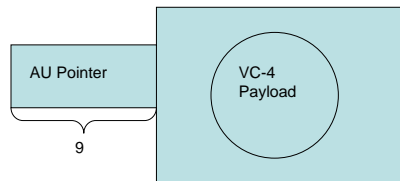
- H1, H2 – Together are used to give the offset of the VC-4 in the STM-1 frame.



- N- New data flag, 1001 – enabled, 0110 – disabled
- I – Increment bit, In positive justification 'I' bits are inverted
- D – Decrement bit, In negative justification D bits are inverted.
- SS – 10
- H3 – Negative justification opportunity bytes
- Y – 1001SS11
- 1* - all 1 bits



AU Pointer

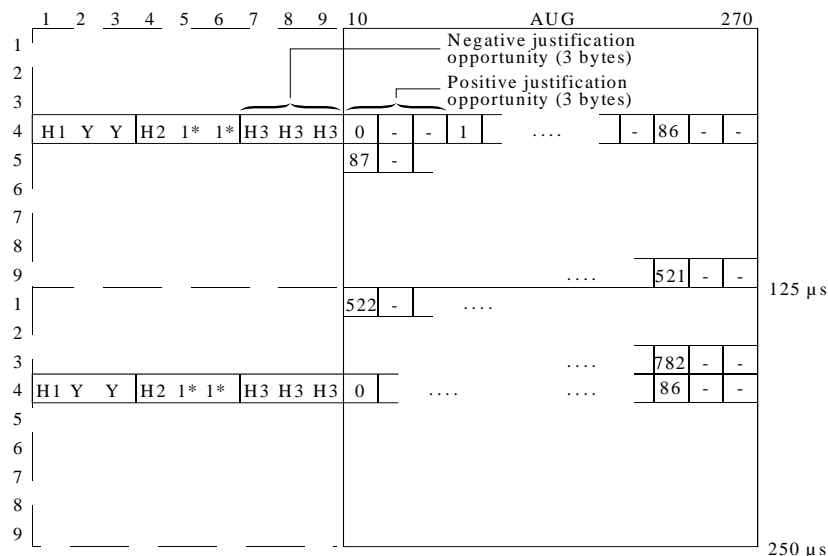


Observations:

- When the payload is directly filled by 140 Mbps PDH an AU pointer will direct to the starting point of VC-4.
- If the VC-4 is filled by lower tributaries such as 34 Mbps, 2 Mbps or any of these two combinations, the AU pointer will not be filled by any information.

65

AU-4 Pointer offset numbering



- The AU-4 pointer value is a binary number with a range of 0 to 782 [to number (261 x 9)/3 bytes] which indicates the offset, in three-byte increments, between the pointer and the first byte of the VC-4 (POH is included in this numbering).
- Numbering starts from the first byte of the 4th row of VC.

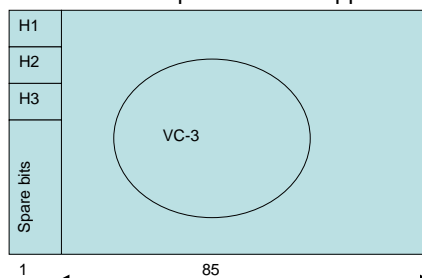
TU3 Pointer

Similar to AU pointer this TU3 pointer will be filled only when the VC-3 is filled directly from PDH 34 Mbps.

If it is filled by 2 Mbps these pointer bytes will not be filled and will be treated as spare.

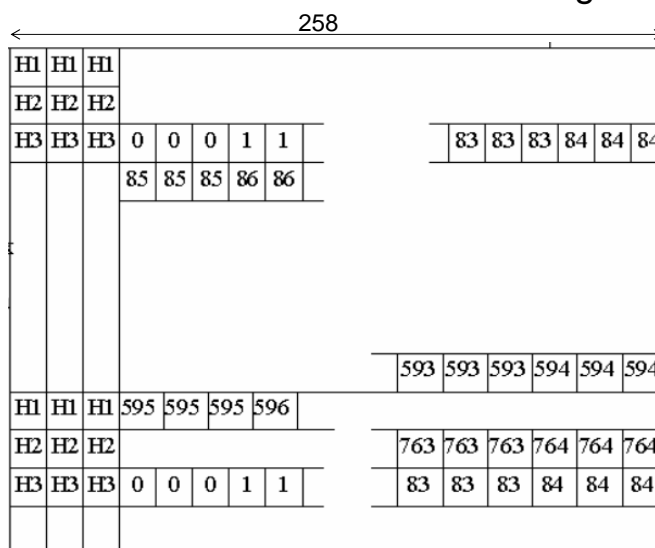
This points to VC-3 within the TU3 frame. Following shows TU3 pointer in the TU3 frame.

TU 4 pointer is similar to TU 3 pointer on its application.



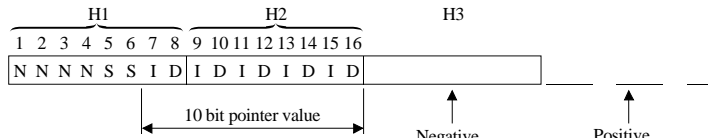
67

TU-3 Pointer offset numbering



The TU-3 pointer value is a binary number with a range of 0-764 $[(255 \times 9)/3]$ which indicates the offset between the pointer and the first byte of the VC-3 (POH is included).

AU-n/TU-3 Pointer (H1, H2, H3) Coding



I Increment
D Decrement
N New data flag

New data flag

- Enabled when at least 3 out of 4 bits match "1001"
- Disabled when at least 3 out of 4 bits match "0110"
- Invalid with other codes

Negative justification

- Invert 5 D-bits
- Accept majority vote

Pointer value (b7-b16)

- Normal range is:
 - for AU-4, AU-3: 0-782 decimal
 - for TU-3: 0-764 decimal

Positive justification

- Invert 5 I-bits
- Accept majority vote

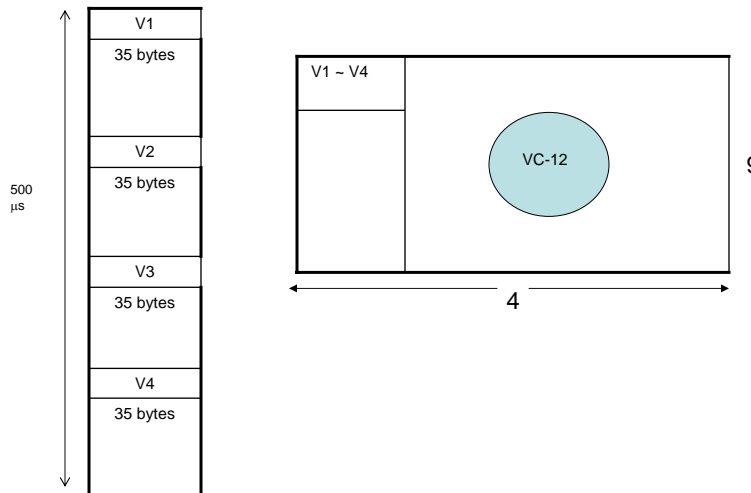
Concatenation indication

- 1001SS1111111111 (SS bits are unspecified)

SS bits	AU-n/TU-n type
10	AU-4, AU-4-Xc, AU-3, TU-3

TU12 Pointer

This points to VC-12 within the TU12 frame. Following shows TU12 pointer in the TU12 frame.



70

TU-12

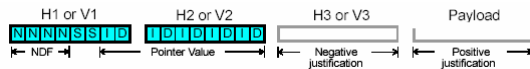
V1
105
⋮
139
V2
0
⋮
34
V3
35
⋮
69
V4
70
⋮
104

TU-12 Pointer offset numbering

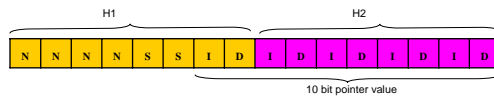
- The TU-12 pointer value contained in V1 and V2 indicates the offset from V2 (V3, V4 bytes are not counted) to the first byte of the VC-12.
- 0-139 which indicates the offset between the pointer and the first byte of the VC-12.
- That is, the value of the pointer for a TU-12 has a range of 0 to 140. For example, if the TU Payload Pointer has a value of 0, then the VC-12 begins in the byte adjacent to the V2 byte; if the TU Payload Pointer has a value of 35, then the VC-12 begins in the byte adjacent to the V3 byte.
- The V5 byte is the first byte of the VC-12 in the first multiframe.

71

Details of the Pointer Coding



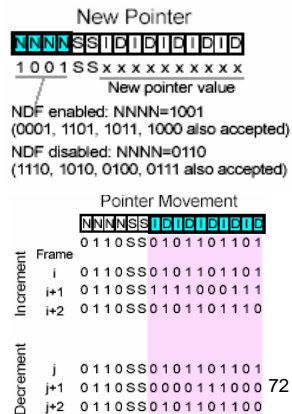
H1, H2 – Together are used to give the offset of the payload.



N- New Data Flag - Bits 1-4 (N-bits) of the pointer word carry an NDF. It is the mechanism which allows an arbitrary change of the value of a pointer. the normal value is "0110", and the value "1001" indicates a new alignment for the VC-n, and possibly new size. 1001 – enabled, 0110 – disabled

I – Increment bit, In positive justification 'I' bits are inverted
 D – Decrement bit, In negative justification D bits are inverted.

SS – 10



Operational Principles of a pointer

- H1 & H2 bytes : Indicates the offset value of the starting of a frame. Offset value can be of 3 types.
 - Offset zero – Zero justification : Frame starts in the normal word number 1.
 - Offset Positive – Positive Justification: Frame starts in the word number n. the value of n will be given in the H1 & H2 bytes.
 - Offset Negative - Negative Justification: Frame start in advance. Starting point will be one of the 9 bytes of the H3.

73

Pointer Summary

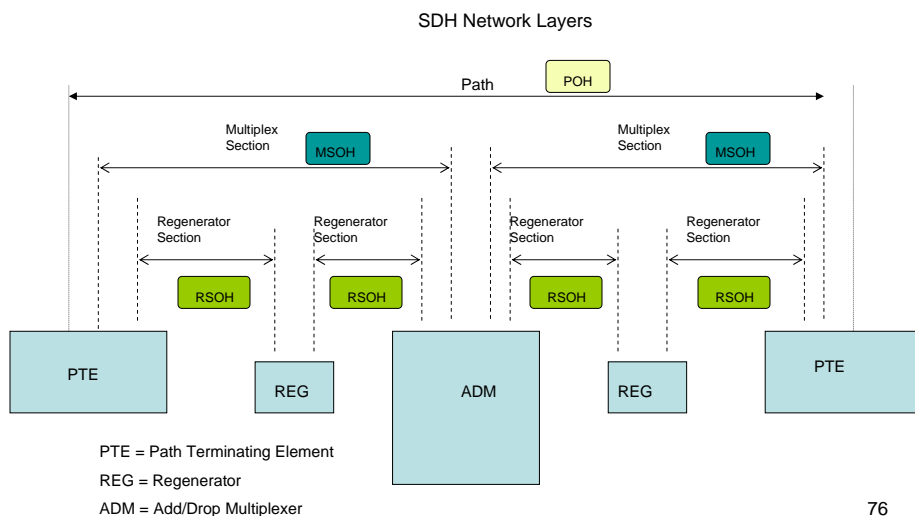
Pointer	AU-4	TU-3	TU-12
	Provides a method of allowing flexible and dynamic alignment of the VC4 within the AU-4 frame.	Provides a method of allowing flexible and dynamic alignment of VC-3 within the TU-3 frame.	Provide a method of allowing flexible and dynamic alignment of the VC-12 the TU-multiframe
Location	Forth row (9 bytes) of Overhead byte section	Contained in TU-3 as three separate H1, H2 and H3 bytes	At the beginning of each frame (4 bytes - V1, V2, V3, V4.
H1, H2 (or V1, V2)	The pointer contained in H1 and H2 designates the location of the byte where the VC 4 begins.	The TU-3 pointer value contained in H1 and H2 designates the location of the byte where the VC-3 begins.	The TU-12 pointer value contained in V1 and V2 indicates the offset from V2 (V3, V4 bytes are not counted) to the first byte of the VC12
N bits - Bits 1-4 of the pointer word	carry an NDF(New Data Flag) which allows an arbitrary change of the pointer value if that change is due to a change in the payload.	Carry an NDF which allows an arbitrary change of the value of the pointer if that change is due to a change in the VC-3.	Carry an NDF. It is the mechanism which allows an arbitrary change of the value of a pointer.
SS bits - two S bits (bits 5 and 6)	Fixed - 01	Fixed - 01	Specify the size /indicate the Tributary Unit type. TU12 – 10
I,D bits - The last ten bits (bits 7-16) of the pointer word	Carry the pointer value.	Carry the pointer value.	Carry the pointer value.
H3 / V3	Negative justification byte appears in the individual H3 byte of the AU-4 frame containing inverted D-bits. A positive justification byte appears immediately after the individual H3 byte of the AU-4 frame containing inverted I-bits	Negative justification byte appears in the individual H3 byte in the TU-3 frame containing inverted D-bits. A positive justification byte appears immediately after the individual H3 byte in the TU-3 frame containing inverted I-bits.	A positive justification opportunity immediately follows the V3 byte. Additionally, V3 serves as the negative justification opportunity such that when the opportunity is taken, V3 is overwritten by data
V4			Reserved
Pointer Value range	0 to 782 which indicates the offset, in three-byte increments, between the pointer and the first byte of the VC-4	0-764 which indicates the offset between the pointer and the first byte of the VC-3	0-139 which indicates the offset between the pointer and the first byte of the VC-12

SDH Major Operational Components

- In SDH basic element is a Virtual Container. This container will follow a specified path from originating node to destination node. Hence a virtual container has to travel a path. When it is traveling its path, it will encounter 2 major operational components.
- These major operational components in the SDH are as follows;
 - Regenerator Unit
 - Add-Drop Multiplexer or Terminal Multiplexer Unit
- The above 2 major components are managed separately from one multiplex unit to the immediate next multiplex unit as a multiplexer section and from a regenerator to the immediate next / previous either multiplex unit or regenerator as a regenerator section.
- When a VC follow a path it will encounter many regenerator sections as well as many multiplexer sections.
- Therefore 3 types of overheads can be identified.
 - In the VC Path Overhead (already analyzed.)
 - Regenerator Section Overhead (RSOH)
 - Multiplexer Section Overhead (MSOH)
- In a multiplexer unit before the analysis of MSOH, RSOH will be checked treating this multiplexer unit as a repeater.

75

Summary of SDH Management Sections

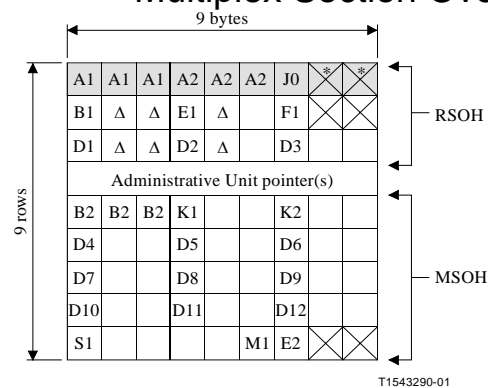


76

- **Regenerator Section Overhead**
 - The Regenerator Section Overhead contains only the information required for the elements located at both ends of a section.
 - The Regenerator Section Overhead is found in the first three rows of Columns 1 through 9 x N of the STM-N, $N \geq 1$ frame.
- **Multiplex Section Overhead**
 - The Multiplex Section Overhead contains the information required between the multiplexer section termination equipment at each end of the Multiplex section.
 - The Multiplex Section Overhead is found in Rows 5 to 9 of Columns 1 through 9 x N of the STM-N, $N \geq 1$ frame.
- **Path Overhead**
 - Discussed earlier

77

STM-1 Regenerator section overhead (RSOH) & Multiplex Section Overhead (MSOH)



T1543290-01

- Unscrambled bytes
- ✕ Bytes reserved for national use
- * The content of these reserved bytes has to be carefully selected as they are not scrambled.
- △ Media-dependent bytes

- A1 and A2 - Framing
- J0 - Regenerator Section (RS) Trace message
- B1 - RS bit interleaved parity code (BIP-8) byte
- E1 - RS orderwire byte
- F1 - RS user channel byte
- D1, D2, D3 - RS Data Communications Channel (DCC) bytes
- B2 - Multiplex Section (MS) bit interleaved parity code (MS BIP-24) byte
- K1 & K2 - Automatic Protection Switching (APS) channel bytes
- D4 to D12 - MS Data Communications Channel (DCC) bytes S1 - Synchronization status message byte (SSMB)
- M1 - MS remote error indication
- E2 - MS orderwire byte

NOTE – All unmarked bytes are reserved for future international standardization (for media-dependent, additional national use and other purposes).

78

Regenerator Section Overhead

- A1 and A2 - Framing bytes – These two bytes indicate the beginning of the STM-N frame. The A1, A2 bytes are unscrambled. A1 has the binary value 11110110, and A2 has the binary value 00101000. The frame alignment word of an STM-N frame is composed of (3 x N) A1 bytes followed by (3 x N) A2 bytes.
- J0 - Regenerator Section (RS) Trace message – It's used to transmit a Section Access Point Identifier so that a section receiver can verify its continued connection to the intended transmitter. The coding of the J0 byte is the same as for J1 and J2 bytes.
- Z0 - These bytes, which are located at positions in STM-N signal (N > 1), are reserved for future international standardization.
- B1 - RS bit interleaved parity code (BIP-8) byte – This is a parity code (even parity), used to check for transmission errors over a regenerator section. Its value is calculated over all bits of the previous STM-N frame after scrambling, then placed in the B1 byte of STM-1 before scrambling.
- E1 - RS orderwire byte – This byte is allocated to be used as a local order wire channel for voice communication between regenerators.
- F1- RS user channel byte – This byte is set aside for the user's purposes; it can be read and/or written to at each section terminating equipment in that line.
- D1, D2, D3 - RS Data Communications Channel (DCC) bytes – These three bytes form a 192 kbit/s message channel providing a message-based channel for Operations, Administration and Maintenance (OAM) between pieces of section terminating equipment. The channel can be used from a central location for control, monitoring, administration, and other communication.

Multiplex Section Overhead

- B2 - Multiplex Section (MS) bit interleaved parity code (MS BIP-24) byte – This bit interleaved parity N x 24 code is used to determine if a transmission error has occurred over a multiplex section. It's even parity, and is calculated overall bits of the MS Overhead and the STM-N frame of the previous STM-N frame before scrambling.
- K1 and K2 - Automatic Protection Switching (APS channel) bytes – These two bytes are used for MSP (Multiplex Section Protection) signaling between multiplex level entities for bi-directional automatic protection switching and for communicating Alarm Indication Signal (AIS) and Remote Defect Indication (RDI) conditions.

K1 Byte	Type of request	K2 Byte	
Bits 1-4		Bits 1-4	Selects channel number
– 1111	Lock out of Protection	Bit 5	Indication of architecture
– 1110	Forced Switch	0	1+1
– 1101	Signal Fail – High Priority	1	1:n
– 1100	Signal Fail – Low Priority	Bits 6-8	Indicate mode of operation
– 1011	Signal Degrade – High Priority	111	MS-AIS
– 1010	Signal Degrade – Low Priority	110	MS-RDI
– 1001	(not used)	101	Provisioned mode is bi-directional
– 1000	Manual Switch	100	Provisioned mode is unidirectional
– 0111	(not used)	011	Future use
– 0110	Wait-to-Restore	010	Future use
– 0101	(not used)	001	Future use
– 0100	Exercise	000	Future use
– 0011	(not used)		
– 0010	Reverse Request		
– 0001	Do Not Revert		
– 0000	No Request		
Bits 5-8	Indicate the number of the channel requested		

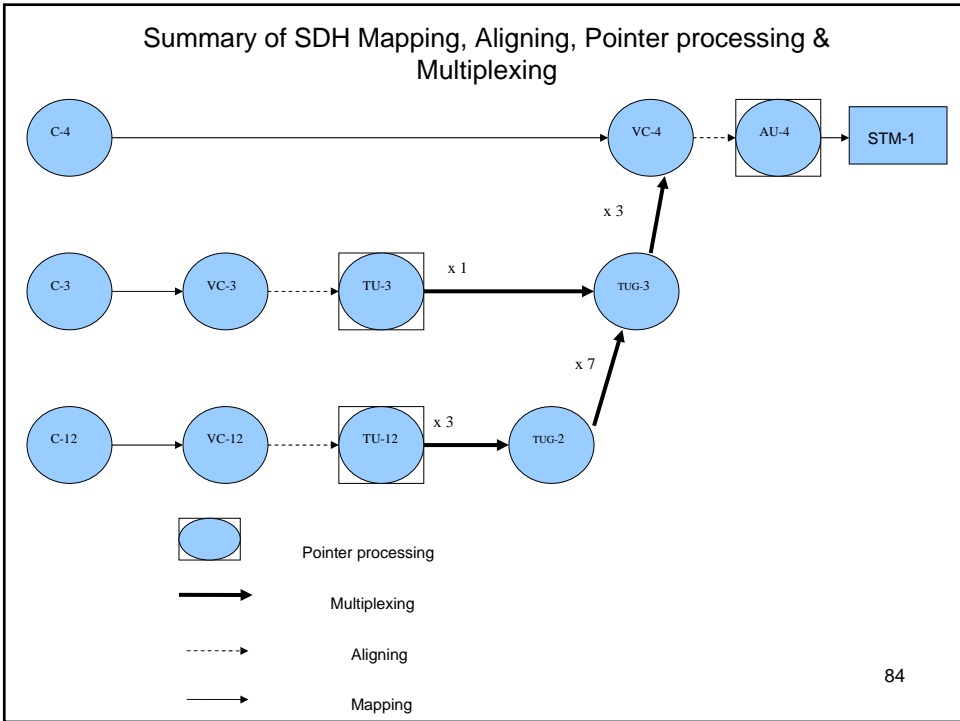
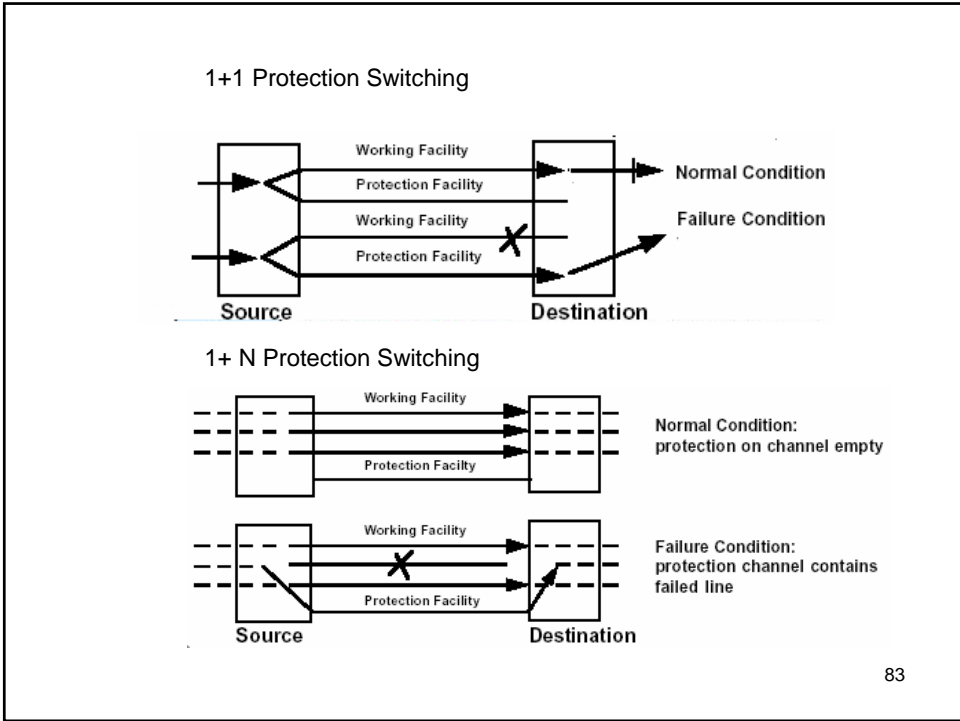
80

Multiplex Section Overhead (contd.)

- D4 to D12 - MS Data Communications Channel (DCC) bytes – These nine bytes form a 576 kbit/s message channel from a central location for OAM information.
- S1- Synchronization status message byte (SSMB) – Bits 5 to 8 of this S1 byte are used to carry the synchronization messages.
 - Bits 5-8
 - 0000 Quality unknown (existing sync.network)
 - 0010 G.811 PRC
 - 0100 SSU-A (G.812 transit)
 - 1000 SSU-B (G.812 local)
 - 1011 G.813 Option 1 Synchronous Equipment Timing Clock (SEC)
 - 1111 Do not use for synchronization. This message may be emulated by equipment failures and will be emulated by a Multiplex Section AIS signal.
- M1- MS remote error indication – The M1 byte of an STM-1 or the first STM-1 of an STM-N is used for a MS layer remote error indication (MS-REI).
- E2 - MS orderwire byte – This orderwire byte provides a 64 kbit/s channel ⁸¹ between multiplex entities for an express orderwire.

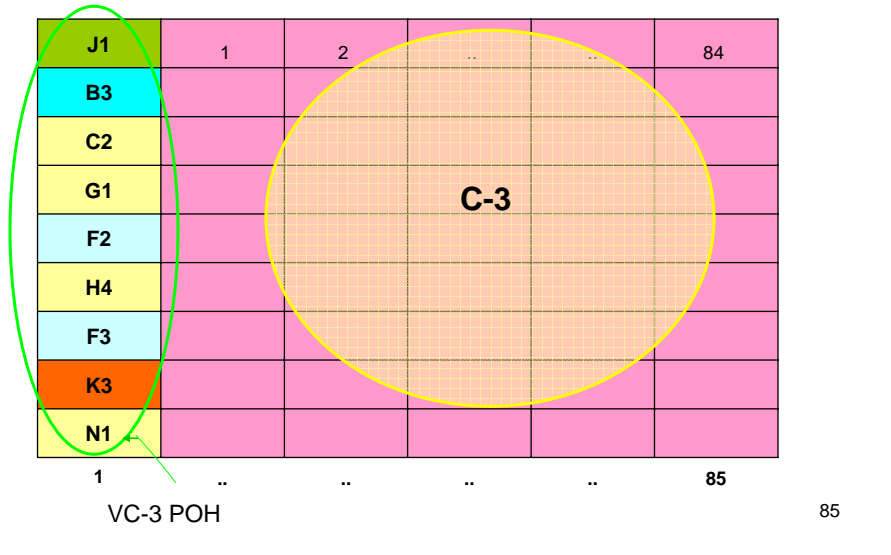
Automatic Protection Switching (APS)

- Automatic Protection Switching (APS) is the capability of a transmission system to detect a failure on a working facility and to switch to a standby facility to recover the traffic.
- This capability has a positive effect on the overall system availability.
- Two modes of APS are provided:
 - 1+1 protection switching
 - 1:N protection switching.



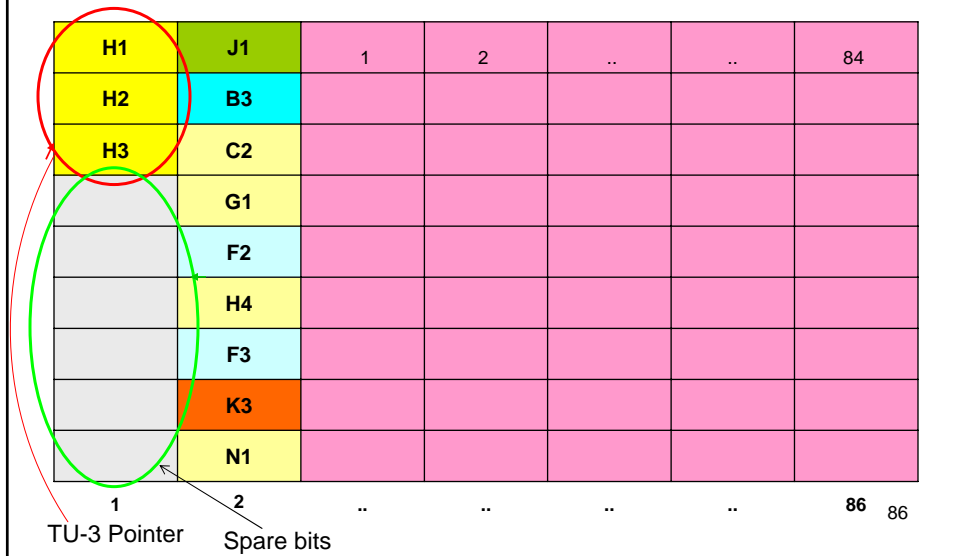
VC-3 Structure

When mapped by 34Mbps or 44Mbps

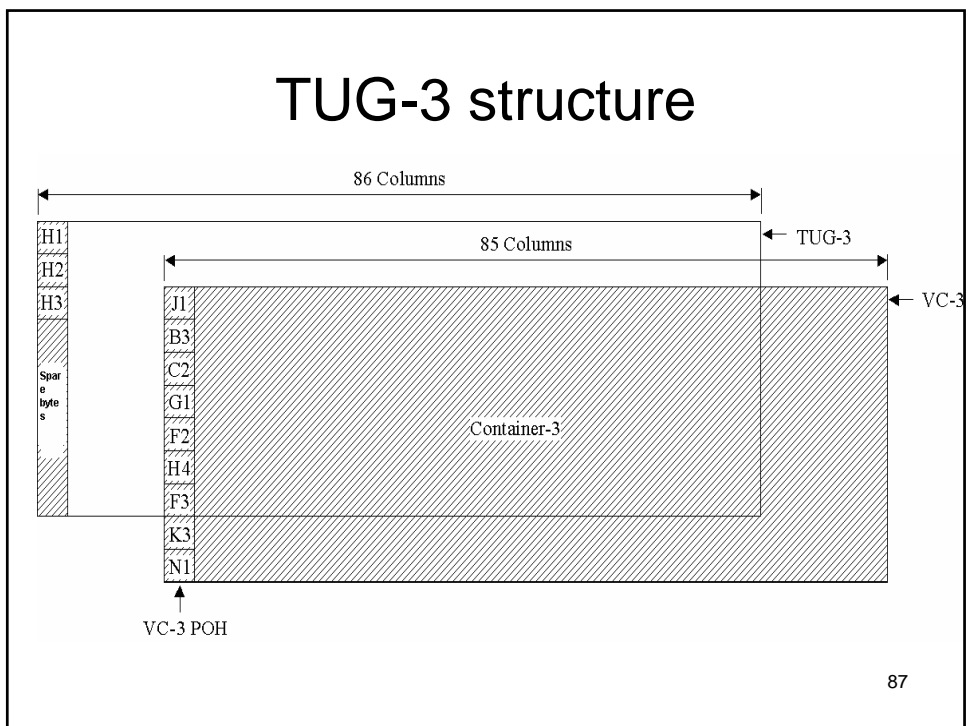


TUG-3 Structure

When mapped by 34Mbps or 44Mbps



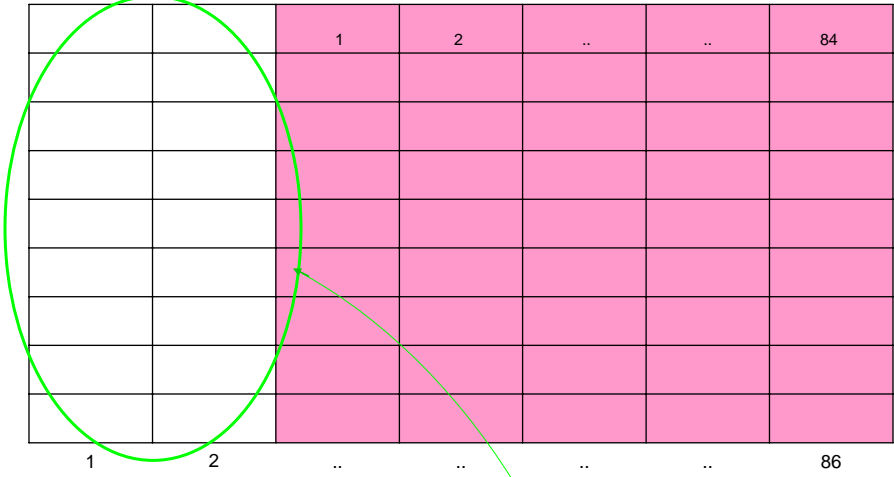
TUG-3 structure



87

TUG-3 Structure

When mapped from lower order



* - no POH are added at VC3, but the individual POHs will be carried by each lower order container, i.e. VC12

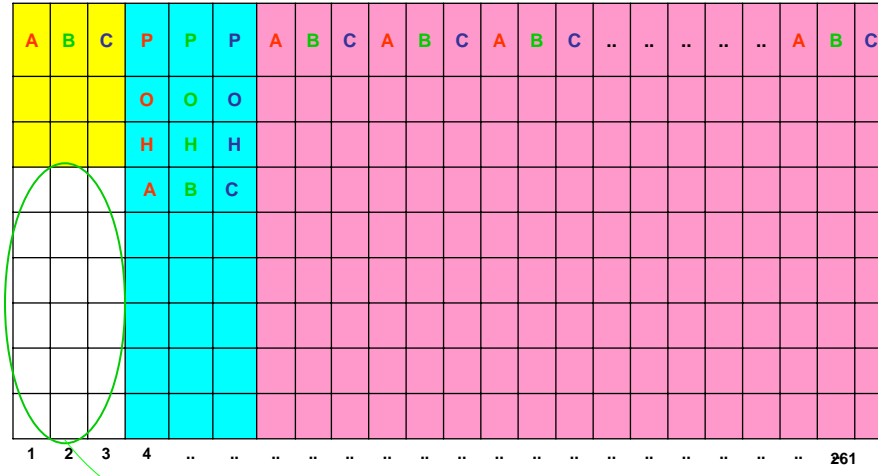
Spare bits

88

Structure of VC4

When mapped from TUG3:

TUG x 3 (A,B,C)= AU4

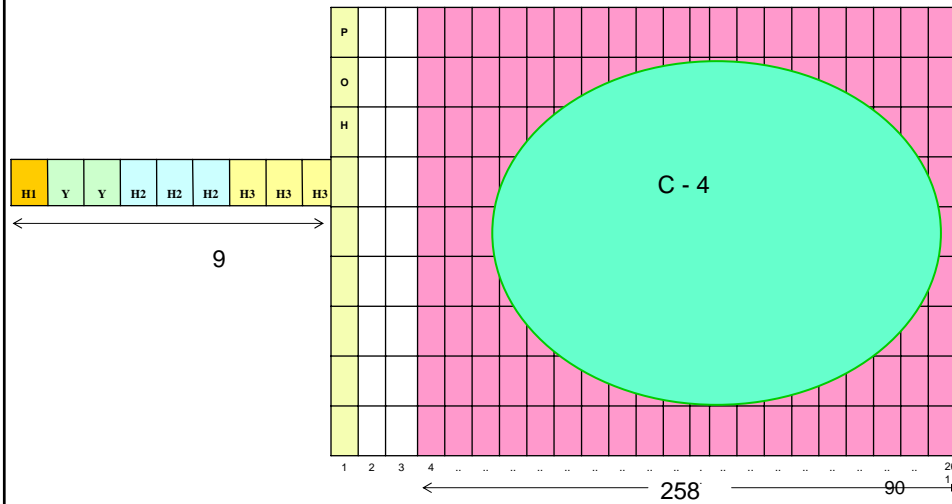


Spare bits

89

Structure of AU4

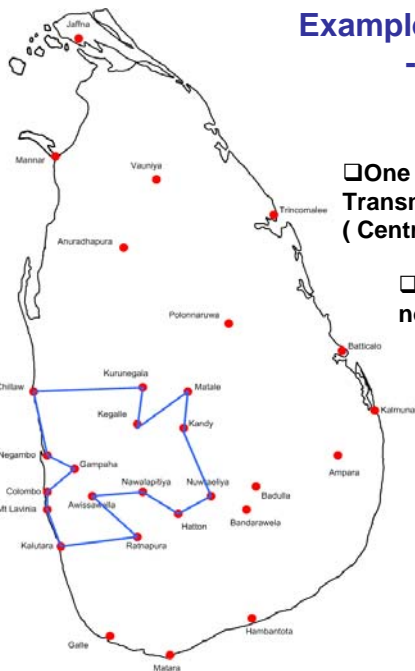
When mapped from VC4:



Examples of SDH Networks

91

Examples of Local SDH Network - SLT Central Ring



□ One High speed (STM-16) OF Transmission network is available. (Central Ring)

□ Optical Fiber cable failure between two nodes does not cause any traffic loss

□ Present Availability of this ring is 99.955%

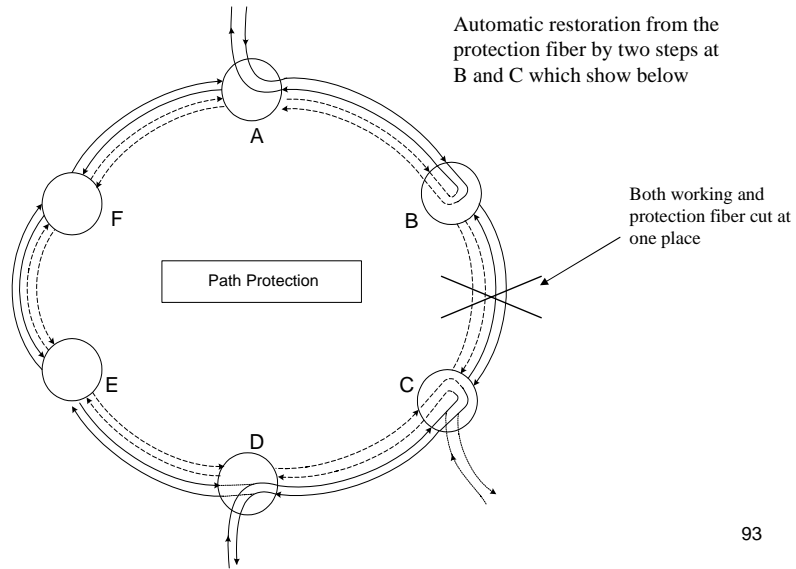
□ Availability of this ring will be 100% soon

□ 700km in length

□ This ring caters only a part of SLT network

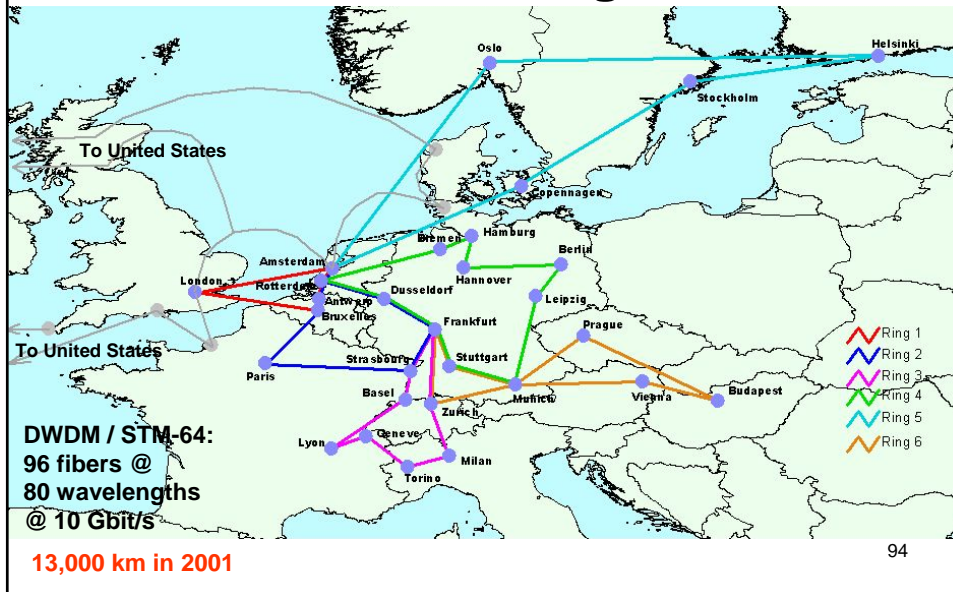
92

Principle of Self-Healing in an SDH Ring Network



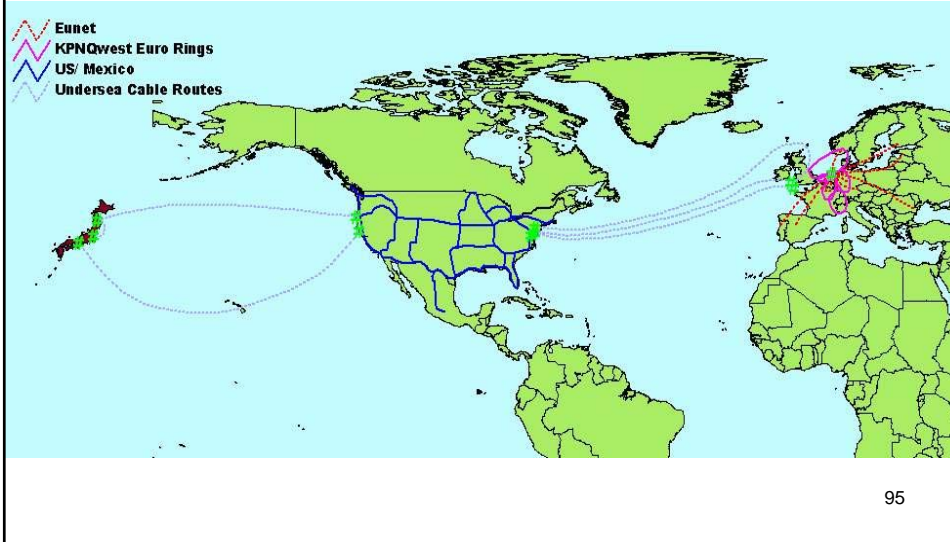
93

Examples of Global SDH Network KPNQwest EuroRings Network

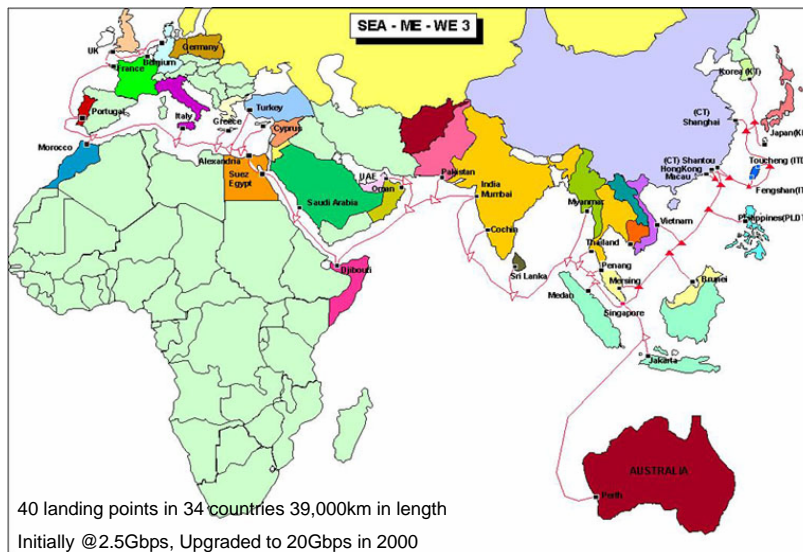


94

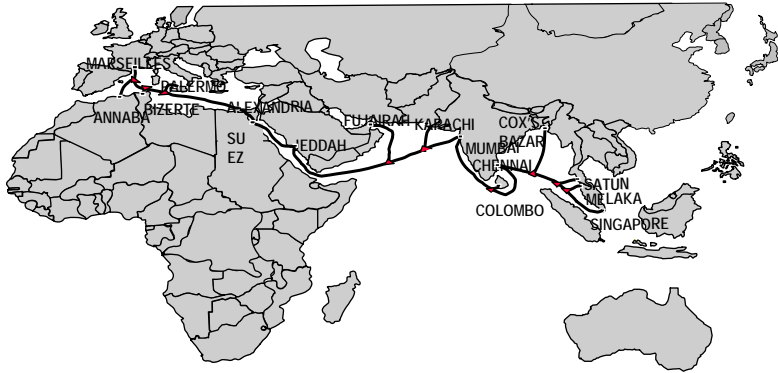
Examples of Global SDH Network Qwest Unified Global Broadband Network



Examples of Global SDH Network SEA ME WE3



Examples of Global SDH Network SEA ME WE4



20,000km long Ultimate
capacity 1.2Tbps

97

Examples of Global SDH Network



98

Examples of Global SDH Network

- US / Mexico
- KPNQwest EuroRings
- EUNET
- Undersea Cable Routes



99

100